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SINGLE-PHASE ELECTRONIC LOAD INTERACTIONS WITH SUPPLY NETWORK

Master of Science Thesis

Examiner: Professor Teuvo Suntio
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ABSTRACT

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Small power electronic loads are becoming more and more common to improve efficiency and provide power to load apparatus with good regulation. The EMC standards for harmonic current emissions apply when the rated power in standard is exceeded. In most cases, the sinusoidal voltage has to be rectified for the load, which creates harmonic currents depending on the implementation of the rectifier. The low power applications use the cheapest diode bridge rectifier, which creates highly distorted currents. These currents reduce power factor and cause neutral currents to appear in three-phase systems. Active power factor correction is needed with higher power loads to comply with the standards.

The main problems caused by the electronic loads are the harmonic current emissions, high frequency interference and the constant input power. One small power device does not cause any problems in a stiff network but the situation may change when the share of problematic loads keeps increasing. While incandescent lights are being replaced with energy saving lamps, the share of small power electronic loads in the network is increasing rapidly. It is well known that the incandescent bulbs are resistive loads causing no problems with electric quality. Energy saving lamps and various other electronic loads are characterized to clarify the electrical properties of common household devices.

The interaction of power line communication and electronic loads can be harmful for the communication, which is used e.g. with automatic meter reading. High frequency switching noise from the neighboring devices and interactions with communication signal and load impedance can lead to corrupted data. The load impedances can potentially cause also stability problems. Converters, which regulate their output, operate with constant power. When the voltage in the network drops, the devices draw more current to maintain the power, which may cause high currents and oscillations in the network during the voltage dip caused e.g. by a fault in the power grid. The stability of an interconnected system can be defined by analyzing source and load impedances at the interconnection point. The validity of the impedance-ratio based stability criterion is also demonstrated in this thesis.

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Nykyisen energiansäästökampanjan aikana tehoelektroniikan merkitys on kasvanut huomattavasti ja tulee yhä kasvamaan. Tehoelektroniikan avulla voidaan toteuttaa energiatehokkaita teholähteitä ja järjestelmiä. Ilman tehoelektroniikkaa myös uusiutuvien energialähteiden hyödyntäminen olisi hankalaa tai jopa mahdotonta. Esimerkiksi aurinkosähköjärjestelmien liittäminen verkkoon vaati tehoelektroniikalla toteutetun liitäntälaitteen. Tehoelektroniikkalaitteiden lisääntyessä myös niille tyypilliset haittavaikutukset lisääntyvät. Korkeaan kytkentätaajuuteen perustuva toiminta aiheuttaa suuritaajuisia virta- ja jännitekomponentteja, jotka voivat häiritä esimerkiksi kommunikaatiolaitteita. Tehoelektroniikkalaitteet ovat myös hyvin dynaamisia laitteita, joka täytyy ottaa huomioon järjestelmiä suunniteltaessa luotettavan toiminnan takaamiseksi. Tässä diplomityössä tutkitaan tavallisten yksivaiheisten elektronisten kuormien sähköisiä ominaisuuksia ja mahdollisia haittavaikutuksia sähkön laadun kannalta.

Elektroniset kuormat tarkoittavat sitä, että sähköverkon jännite muutetaan kuormalle sopivaan muotoon. Lähes aina tämä tarkoittaa vaihtojännitteen tasasuuntausta, jonka jälkeen se vielä reguloidaan toimilaitteelle sopivaksi. Tasasuuntauksesta riippuu, kuinka paljon laitteen ottama virta säröytyy. Passiivinen dioditasasuuntaus tuottaa erityisen paljon niin sanottuja virran harmonisia yliaaltokomponentteja, jotka aiheuttavat ylimääräisiä häviöitä johtimissa ja muuntajissa sekä laskevat tehokerrointa, sillä vain perustaajuinen komponentti siirtää pätötehoa. Kolmella jaolliset yliaallot eivät myöskään summaudu nollaksi kolmivaihejärjestelmässä, jolloin nollajohtimen virta voi kasvaa jopa noin 1,7-kertaiseksi yhden vaiheen virtaan nähden. Tästä voi aiheutua ongelmia, sillä nollajohdin mitoitetaan yleensä vaihejohtimien suuruiseksi tai jopa pienemmäksi. Suurimmasta osasta harmonisia virtoja voidaan päästä eroon käyttämällä aktiivista tehokertoimen korjausta (PFC).

Standardi EN 61000-3-2 määrittelee kuinka säröytynyttä laitteen ottama virta saa olla. Standardi on jaettu neljään luokkaan. Luokkaan A kuuluu suurin osa tavallisista kotitalouskojeista, paitsi valaisimet, jotka kuuluvat luokkaan C sekä

tietokoneet, näytöt ja televisiot, jotka kuuluvat luokkaan D. Luokkaan B kuuluu esimerkiksi kannettavia työkaluja. Yleisesti rajat koskevat laitteita joiden teho on 75W tai enemmän. Pienempitehoisilla laitteilla määräyksiä ei ole. Poikkeuksena C-luokan laitteet, joilla tehoraja on 25W. Myös tätä pienempitehoisilla valaistuslaitteilla on lievät rajat, joihin voidaan päästä passiivisella diodisiltatasasuuntauksella. Käytännössä aktiivista tehokertoimen korjausta joudutaan käyttämään kun tehoraja ylittyy. Pienempitehoisilla laitteilla käytetään lähes poikkeuksetta halvinta mahdollista ratkaisua, eli diodisiltaa, koska laitteen ottaman virran laadusta ei tarvitse välittää.

Erityisen mielenkiintoisia kuormia ovat energiansäästölamput, sillä ne tulevat korvaamaan resistiiviset, sähkön laadun kannalta täysin ongelmattomat hehkulamput. Aluksi kielletään 100W hehkulamput syyskuussa 2009, ja kaikki hehkulamput vuoteen 2013 mennessä. Motivan mukaan Suomessa oli vuonna 2007 yli 45 miljoonaa keskimäärin 58W hehkulamppua. Kyseessä on siis huomattavan kokoinen kuorma. 60W hehkulamput korvataan yleensä 11W energiansäästölampuilla, joten idea kuulostaa erinomaiselta energian säästön kannalta. Vaikutukset sähkön laatuun ovat kuitenkin jääneet vähäiselle huomiolle. Työssä 11W energiansäästölampuista on mitattu korkeita virran säröarvoja, pieni tehokerroin (kapasitiivinen) ja noin 1,7-kertainen nollajohtimen virta vaihevirtaan nähden, kun kolmivaihejärjestelmään laitettiin samanlainen viiden lampun kuorma jokaiseen vaiheeseen.

Automaattinen sähkömittareiden luenta (AMR) on tulossa yhä tärkeämmäksi osaksi sähköyhtiöiden toimintaa. Usein AMR toteutetaan jo valmista sähköverkkoa hyväksikäyttäen. Verkon vaihtojännitteeseen moduloidaan suurtaajuinen jännitekomponentti tiedonsiirtoa varten. Tämän jännitekomponentin reagoidessa esimerkiksi diodisiltatasasuuntaajien kondensaattoreiden ja verkon induktanssien aiheuttamien resonanssien kanssa syntyy suuritaajuisia virtoja, joka vaimentaa tiedonsiirtosignaalia. Tätä pidetään jopa suurimpana ongelmana sähköverkkoa käyttävän tiedonsiirron kanssa. Myös kytkentätaajuiset häiriökomponentit vaikeuttavat tiedonsiirtoa. Standardeissa ei oteta huomioon sähköverkon kautta mahdollisesti tapahtuvaa tietoliikennettä.

Yhä useammat laitteet pystyvät toimimaan hyvin suurella jännitealueella, jopa 80-270V. Valmistajan kannalta tämä on logistisesti edullista, sillä samaa tuotetta voidaan markkinoida globaalisti. Usein tällaiset laitteet ovat esimerkiksi matkapuhelinten latureita sekä kannettavien tietokoneiden teholähteitä, jollaiset myös tässä työssä on mitattu. Ongelmana tällaisten laitteiden kanssa on juuri vakiotehoinen toiminta laajalla jännitealueella. Jännitekuopan aikana kyseiset laitteet toimivat edelleen vakioteholla, josta voi olla seurauksena huomattavaa virtojen kasvua verkostossa, kun yhä useammat laitteet ottavat lisää virtaa säilyttääkseen vakiotehon ja ongelmia voi aiheutua verkon mitoituksen kanssa. Vakioteholaitteiden dynaaminen vuorovaikutus syöttävän lähteen kanssa voi aiheuttaa myös värähtelyä ja stabiilisuusongelmia.

Vakioteholaitteiden sisääntulossa näkyy niin sanottu dynaaminen negatiivinen resistanssi, joka riippuu toimintapisteessä. Negatiivinen resistanssi tarkoittaa sitä, että jännitteen laskiessa virta nousee, eli päinvastoin kuin resistanssin tapauksessa.

Negatiivinen resistanssi nähdään taajuustason impedanssista taajuusalueella, jolla laitteen säätöjärjestelmä pystyy reguloimaan ulostulonsa sisääntulon muutoksista riippumatta. Negatiivisen resistanssin vaikutuksesta kuorman sisääntuloimpedanssin vaihe siis laskee -180 asteeseen matalilla taajuuksilla. Yhteenkytketyn, lähteen ja kuorman muodostaman järjestelmän stabiilisuus voidaan määrittää tarkastelemalla impedansseja liityntäpisteessä. Jos lähteen ulostuloimpedanssin Z_o ja kuorman sisääntuloimpedanssin Z_{in} suhde $Z_o/Z_{in}=-1$ (vahvistukset yhtä suuret ja vaihe-ero 180˚), on järjestelmä epästabiili. Luonnollisesti kuorman vaiheen laskeminen -180 asteeseen lisää epästabiiliuden riskiä. Epästabiilius voi aiheutua esimerkiksi mahdollisesta verkon LC-resonanssista kuormien negatiivisen resonanssin dominoimalla alueella.

Vakiotehoisia kuormia ovat esimerkiksi aktiivisella tehokertoimen korjauksella varustetut laitteet ulostulonsa jännitesäädön takia, sekä diodisillalla varustetut laitteet, joissa diodisillan perässä on DC-DC hakkuri reguloimassa kuormajännitettä. Kaikista vakioteholähteistä mitattiin negatiivisen resistanssin ominaisuuksia matalilla taajuuksilla. Diodisillan kautta syötettyjen energiansäästölamppujen teho laskee jännitteen laskiessa, mutta siitä huolimatta myös niistä mitattiin negatiivisen resistanssin ominaisuuksia, joka aiheutuu lamppupiiriä syöttävän resonanssi-invertterin ja loistelampun ominaisuuksista. Useista diodisiltakuormista mitattiin myös tasavirtakomponentti, joka voi aiheuttaa esimerkiksi muuntajien ja kuristimien sydänmateriaalin saturoitumista.

Markkinoiden tiukan kilpailutilanteen vuoksi erityisesti kuluttajalaitteet tehdään mahdollisimman halvalla, jolloin sähkön laatuun ei kiinnitetä huomiota kuin sen verran, että standardien asettamiin rajoihin päästään juuri ja juuri. Tämä näkyy erityisesti laitteiden ottaman virran harmonisten määrässä. Hehkulamppujen korvaamisen mielekkyys voidaan kyseenalaistaa sähkön laadun kannalta, jos haitat muodostuvat etuja suuremmiksi vaikka energiansäästö onkin jalo tavoite. Tilannetta voitaisiin parantaa tiukentamalla standardeja, mutta tämä lisäisi tehokerrointa korjaavien laitteiden määrää, jolloin erityisesti energiansäästölamppujen negatiivisen resistanssin alue kasvaisi ja epästabiiliuden riski olisi suurempi. Nyky-yhteiskunta on niin riippuvainen sähköstä, että kaikki sähköverkkoa mahdollisesti vaarantavat toimenpiteet tulisi kyseenalaistaa ja tutkia huolellisesti ennen käyttöönottoa.

PREFACE

This thesis has been done at the Department of Electrical Energy Engineering at Tampere University of Technology during the winter 2008-2009 and spring 2009. I would like to thank Professor Teuvo Suntio for the thesis subject and for the valuable instructions and guidance during the thesis. I would also like to thank M.Sc. Jari Leppäaho for the help with measuring equipment and everyone at the Department of Electrical Energy Engineering for the nice working environment. Also greetings to all relatives and friends who might be reading this, thank you for your support.

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LARI NOUSIAINEN

CONTENTS

SYMBOLS AND ABBREVIATIONS

SYMBOLS

η	Efficiency
φ	Phase angle between voltage and current
ω	Angular frequency
ω_p	Angular frequency of pole
ω_z	Angular frequency of zero
c	Control variable
C	Capacitor, capacitance
D, d	Duty ratio
D', d'	Complement of duty ratio
f_s	Switching frequency
G_a	Modulator gain
G_{ca}	Current compensator transfer function
G_{cc}	Controller transfer function
G_{ci}	Control-to-input transfer function
G_{co}	Control-to-output transfer function
$G_{io\text{-}o}$	Line-to-output transfer function
$H_v(s)$	Output-voltage sensing gain
I, i	Current
i_C	Capacitor current
i_{in}	Input current
i_L	Inductor current
i_o	Output current
K, K_f	Gain
L	Inductor, inductance, transfer function
$L(s)$	Loop gain
P	Active power
P_{in}	Input power
R	Resistance
r_C	Capacitor series resistance
r_D	Diode series resistance
r_L	Inductor series resistance
R_s	Inductor current sensing resistor, source resistance
S	Apparent power, transfer function, switch
s	Laplace variable
T, t	Time
$T_{oi\text{-}o}$	Output-to-input transfer function
t_{off}	Switch off-time

t_{on}	Switch on-time
U, u	Voltage
u_C	Capacitor voltage
U_D	Diode voltage loss
u_{in}	Input voltage
u_L	Inductor voltage
u_o	Output voltage
u_r, u_{ref}	Reference voltage
u_{rec}	Full-wave rectified input voltage
v_c	Control voltage
Y_{in}	Input admittance
$Y_{in\text{-}c}$	Closed loop input admittance
$Y_{in\text{-}o}$	Open loop input admittance
Z_{in}	Input impedance
$Z_{in\text{-}c}$	Closed loop input impedance
$Z_{in\text{-}o}$	Open loop input impedance
Z_L	Load impedance
Z_o	Output impedance
Z_{of}	Filter output impedance
$Z_{o\text{-}o}$	Open loop output impedance
Z_S	Source impedance

ABBREVIATIONS

AC	Alternating Current
ACMC	Average Current Mode Control
AM	Amplitude Modulation
AMR	Automatic Meter Reading
CBW	Control Bandwidth
CCM	Continuous Conduction Mode
CFL	Compact Fluorescent Light
CM	Common Mode
CPL	Constant Power Load
DC	Direct Current
DCM	Discontinuous Conduction Mode
DM	Differential Mode
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESL	Energy Saving Lamps
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transform
GM	Gain Margin

IVFF	Input Voltage Feedforward
PCMC	Peak Current Mode Control
PE	Protective Earth
PF	Power Factor
PFC	Power Factor Correction
PID	Proportional-Integral-Derivative
PI	Proportional-Integral
PLC	Power Line Communication
PM	Phase Margin
PWM	Pulse Width Modulation
RHP	Right Half Plane
RMS	Root Mean Square
THD	Total Harmonic Distortion
UPS	Uninterruptable Power Supply
VMC	Voltage Mode Control
ZCD	Zero Crossing Detection

1. INTRODUCTION

Increased environmental awareness and the green values have made efficient use of electrical energy one of the most popular topics in electrical engineering. A good example is the energy saving lamps (ESL). Incandescent light bulbs are already banned or are soon to be banned in numerous countries. In Europe, the ban starts on September 2009 from 100W bulbs and covers all the incandescent lamps by year 2013 after the transition period. Energy saving in lighting is a straightforward way to reduce consumption of electrical energy since it practically does not require change in consumer lifestyle. A lot of articles and discussion at the letters-to-editor sections has emerged for and against the energy saving lamps. Mostly the arguments consider heating value of lamps in households or resources used in manufacturing and dispose of the lamps.

The incandescent bulb is a resistive load causing no problems whatsoever in electric quality point of view. The energy saving lamps and all fluorescent lamps with electronic ballast are electronic loads. The voltage is converted from the network to another form suitable for the lamp circuit. This conversion is done as cost effectively as possible to just and just comply with the electric quality standards. In 2007, 45 million incandescent lamps existed in Finland with an average of 58W power [1]. To replace all of them with 11W lamps sounds impressive while trying to reduce consumption of electrical energy and carbon dioxide emissions. Is the matter that simple? Usually when something positive is gained, there will appear drawbacks in other areas.

The initial motivation for this thesis was to study the electrical characteristics of energy saving lamps and other electronic loads and come to a conclusion of their impact on electric quality and possible stability issues with supply. The energy saving lamp is known to have poor power factor and high total harmonic distortion. Sure few lamps won't have any effect on stiff network but what about millions of them? In [2] relatively high voltage distortion was measured from weak network with large-scale installation of energy saving lamps. To reduce the harmonic distortion, power factor correcting (PFC) devices can be used. They force the input current to track the shape of input voltage to achieve unity power factor and low current harmonic distortion. These power electronic devices are used e.g. as an active front end in higher power fluorescent lamp electronic ballasts [3].

Power electronic devices have important role in energy efficiency and utilization of clean energy resources. The connection of renewable energy resources, e.g. solar panels, to power grid is not possible without power electronics. Electric motor drives, lighting applications, hybrid and electric vehicles and high efficiency power supplies

have high potential in energy saving with intelligent power electronics. It has been estimated that by year 2015 up to 80% of electrical energy is controlled by power electronic systems to improve efficiency [4]. The power electronic systems are able to maintain desired conditions for the load with high precision. When power is maintained constant, the input impedance will show negative incremental resistance characteristics (i.e. when input voltage drops, the input current rises). Accordingly a constant-power-load (CPL)-infected network will experience high currents during the voltage dips.

Constant-power-load related stability issues in distributed AC systems are discussed e.g. in [5] and the issues with regulated DC systems have been studied since the 1970's [6]. Negative resistance instability is a known phenomenon and may cause system oscillations or voltage collapse. Instability has been reported e.g. with aircraft, spacecraft and ship power systems [7]. Besides electric quality discussion, another objective in this thesis is to reveal the negative incremental resistance characteristics of single phase electronic loads in frequency domain and discuss the effect of CPLs to stability. Also high frequency interference of electronic loads with communication technologies utilizing power grid is discussed.

The rest of the thesis is organized as follows. Chapter 2 makes a summary to common electromagnetic compatibility (EMC) issues of electronic loads, stability analysis and discusses input impedance. Chapter 3 is meant as a brief review to modeling power electronic devices and as illustration for the source-load stability issue. In Chapters 4 and 5 Simulink models are built for load with active power factor correction and passive diode rectification, respectively. Also simulation results are represented. Chapter 6 contains measurement data and main conclusions are drawn together in the last chapter.

2. ELECTRONIC LOADS

An electronic load is a load which has active power conversion. Passive loads consist of passive components (resistive, inductive and capacitive). With AC input devices the power is usually converted to DC and then regulated to load with switched mode converter to ensure energy efficient operation. When output voltage or current is kept constant despite of changes in the input, the load operates at constant power. As a consequence the load has optimal conditions but the stability with the source is compromised. The source-load interaction mechanisms are valid with all interconnected systems but the stability issue is emphasized with constant power operation. Traditionally this has been considered as an issue of the converter and its EMI (electromagnetic interference) filter [6] or in distributed power systems [5, 8].

The electronic load front end is mainly subject to regulations and an EMI-filter needs to be used in most cases. Low power applications use diode bridge front end which distorts input currents. The distorted current is a sum of its Fourier series components containing high frequency currents and causes neutral currents in three phase systems to appear as will be discussed later. The switched mode converters are also known for their EMC issues. The high frequency components expose electrical equipment to high frequency interference. A case where radiotelephones could not be used indoors after large-scale installation of energy saving lamps is reported in [9].

Power line communications (PLC) has been designed to be used for example with home automation, local area networks and automatic meter reading (AMR), which is becoming increasingly important in the utilities sector [10]. The frequency bands are located at a wide range (kHz-MHz carriers) depending on application. Any resonance (e.g. caused by EMI-filter) in the load input impedance at the communication frequency may cause large high frequency currents to appear. Combined with power supply switching noises and high frequency harmonics the result is easily corrupted data [11].

2.1. Harmonic Currents

The standard EN 61000-3-2 defines the limits for harmonic current emissions for equipment with input current of 16A or less per phase. The equipment in standard is classified in four classes (A, B, C and D). Class A considers balanced three-phase equipment, household appliances (excluding class D equipment), tools (excluding portable tools), dimmers for incandescent lamps and audio equipment. Class B covers portable tools and nonprofessional arc welding equipment. In class C, the limits are defined for lighting equipment and in class D for personal computers, displays and television sets. In classes A, B and D, the limits apply only to equipment with rated

power of 75W or more. Class C has limits both for equipment with over 25W of rated power and for equipment with rated power of 25W or less. In practice, active power factor correction needs to be used to comply with the limits if rated power in standard is exceeded. The low power limits in class C can be achieved with passive solutions.

The limits are basically given in the Table 2.1: The class A harmonic limits are given in Table 2.1a. The class B equipment harmonic currents shall not exceed the Table 2.1a limits multiplied by a factor of 1.5. The limits for class C equipment with over 25W of rated power are given in Table 2.1b. Class D limits are defined in Table 2.1c. Discharge lighting equipment with active power of 25W or less shall comply with one of the following two sets of requirements:

1) The harmonic currents shall not exceed the power-related limits given in Table 2.1, column 4.

2) The third harmonic current shall not exceed 86% of fundamental current and fifth harmonic shall not exceed 61%. Also the waveform of the input current shall begin at 60˚ or before and shall have its last peak at 65˚ or before and the current shall not stop flowing before 90˚, where the zero crossing of the fundamental supply voltage is at 0˚.

Table 2.1. *Harmonic current limits in EN 61000-3-2.*

a, b, c	a	b	c	
Harmonic order (n)	*Max harmonic current (A)*	*Max harmonic current, percentage of fundamental current (%)*	*Max harmonic current per watt (mA/W)*	*Max harmonic current (A)*
Odd harmonics				
3	2.30	30·PF	3.4	2.30
5	1.14	10	1.9	1.14
7	0.77	7	1.0	0.77
9	0.40	5	0.5	0.40
11	0.33	3	0.35	0.33
13	0.21	3	0.30	0.21
15≤n≤39	0.15·15/n	3	3.85/n	0.15·15/n
Even harmonics				
2	1.08	2	-	-
4	0.43	-	-	-
6	0.30	-	-	-
8≤n≤40	0.23·8/n	-	-	-

With sinusoidal waveforms active power is a product of current, voltage and the cosine of their phase difference. The power factor is defined by the relation of active power and apparent power, according to (2.1). Inverse cosine function (arc-cosine) of the power factor gives the phase angle between sinusoidal current and voltage, as depicted in (2.1).

$$PF = \frac{P}{S} = \frac{U_{RMS} I_{RMS} \cos\phi}{U_{RMS} I_{RMS}} = \cos\phi \tag{2.1}$$

With non-sinusoidal waveforms, the RMS values for voltage and current are defined as the square sum of the waveforms Fourier series frequency component RMS (root mean square) values by

$$U_{RMS} = \sqrt{\sum_{i=1}^{n} U_i^2}\,,\; I_{RMS} = \sqrt{\sum_{i=1}^{n} I_i^2} \tag{2.2}$$

Accordingly, the active power with non-sinusoidal waveforms is derived as a sum of the corresponding frequency component products by

$$P = \sum_{i=1}^{n} U_i I_i \cos\phi_i \tag{2.3}$$

Now the power factor for any waveforms may be represented according to (2.1) as shown in (2.4).

$$PF = \frac{\sum_{i=1}^{n} U_i I_i \cos\phi_i}{\sqrt{\sum_{i=1}^{n} U_i^2} \sqrt{\sum_{i=1}^{n} I_i^2}} \tag{2.4}$$

In case of a stiff supply network, the voltage contains only its fundamental component and active power is delivered only by the fundamental component. Accordingly, the power factor for loads with distorted current and sinusoidal voltage becomes as shown in (2.5) where I_1 / I_{RMS} is known as distortion factor and $\cos\phi_1$ is known as displacement factor, respectively.

$$PF = \frac{U_1 I_1 \cos\phi_1}{U_1 I_{RMS}} = \frac{I_1}{I_{RMS}} \cos\phi_1 \tag{2.5}$$

The current distortion lowers the power factor and limits the maximum available active power. With 16A fuse and load with 0.5 PF, only 8A active current may be delivered to the load. The currents are higher than the rated power suggests. All conductors must be sized to handle all the current flowing in the network not just the active current. The higher the overall current is the higher are the losses in conductors and transformers. This is why unity power factor is optimal, especially, in distribution network. Various compensation equipment [12] and power filters [13] are designed to increase power factor close to unity and low THD (total harmonic distortion) in the network.

In four-wire three phase system, the neutral current is the vector sum of the line-to-neutral currents. Perfectly balanced sinusoidal currents with 120° phase shifts sum to zero at any instance. In three phase system with single phase loads, the imbalance between phase currents tend to exist even with linear loads. Small neutral current in typical slightly unbalanced system causes no problems in common installations. When the line currents are non-sinusoidal, even if perfectly balanced, the neutral current does not sum to zero as visualized in Figure 2.1 [14].

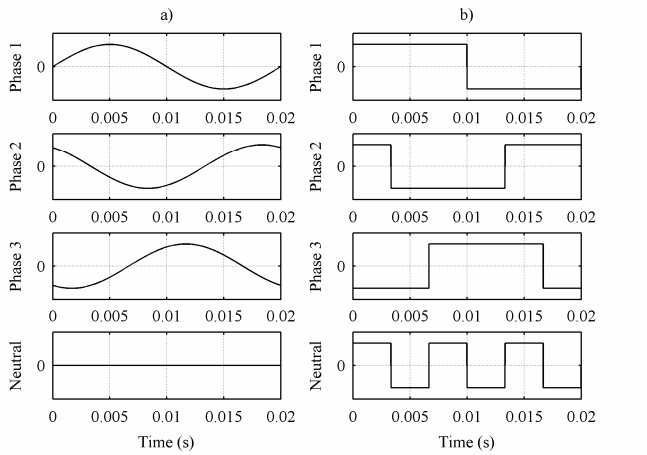


Figure 2.1. *Line and neutral currents in a) balanced three phase sine wave and b) square wave systems.*

The fundamental frequency of the neutral current in square wave system is three times the line frequency (Figure 2.1b). The neutral current composes of the unbalance and triplen harmonics (third, sixth, ninth etc.) [14, 15]. Thus the balanced square wave system neutral current consists only of triplen harmonics, and therefore its fundamental frequency is 150Hz. According to [14], the neutral current may increase up to 1.73 times the line current under worst-case conditions in balanced systems. This should be considered when sizing the neutral conductor. Usually the neutral is sized equal the line conductors or even less. High neutral currents may lead to overloaded conductors and transformers as well as voltage distortion while flowing through supply impedances and common mode noise [14]. Some interesting power system and transformer failures caused by harmonics and neutral currents are reported in [16]. High neutral currents are measured in [17] at computer festivals.

2.2. High Frequency Interference

The high frequency noise in power systems is caused by the harmonic currents and switching noise of electronic loads. In theory, the Fourier series of distorted currents with line frequency fundamental would contain infinite amount of components but in practice the components are limited to relatively low frequencies (e.g. third, fifth, seventh etc.) without additional high frequency source. Switching power electronic equipment is naturally a source of electromagnetic pollution due to rapidly changing voltages and pulsating currents required by the tight and energy efficient power handling [18]. Due to high rate of rise of pulses, the spectrum of currents contains radio frequencies subjected to EMC compliance standards. Generic emission standard for residential, commercial and light industry is defined in standard EN 50081-1. Old immunity standard EN 50082-1 is replaced by EN 61000-6-1. Part 2 of the standards considers industrial environment.

The noise currents caused by pulsating currents are commonly known as differential mode (DM) noise currents. The rapid change in voltage causes easily currents via associated stray capacitances. These currents may add to DM noise currents or may cause currents commonly known as common mode (CM) currents. The CM currents may escape from the equipment via the air by cabling acting as an antenna or trough the grounding (PE-conductor) and possibly cause both conducted and radiated noise. The electromagnetic fields may also escape through the holes in the casing resulting as radiated noise [19]. Filtering is the most common way to suppress the noise escaping from the equipment to acceptable levels defined in the relevant standards.

LC-type filters are the most common filters used. Usually the filter components are modeled with their equivalent series resistances (ESR). If more accurate model is needed all the parasitic elements have to be considered. A small parasitic capacitance is formed between the inductor windings and capacitor has small series inductance like basically any conductor. Usually the resonance frequency ($f_r = 1/2\pi\sqrt{LC}$) of a component can be found from the datasheet. Figure 2.2 presents the LC-filter circuit with all the parasitic elements and with ideal voltage source and current load. Corresponding input impedance frequency responses with resistive parasitic and all parasitic elements are shown in Figure 2.3.

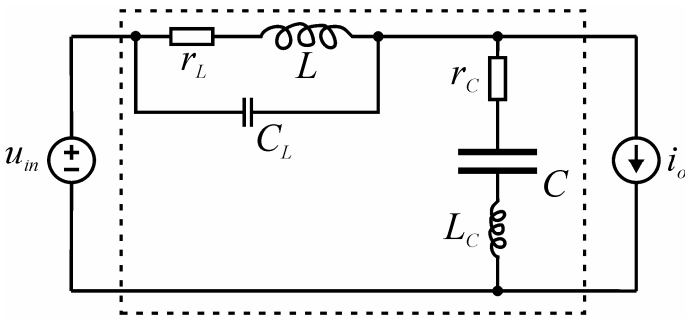


Figure 2.2. *LC-type EMI-filter with all parasitic elements.*

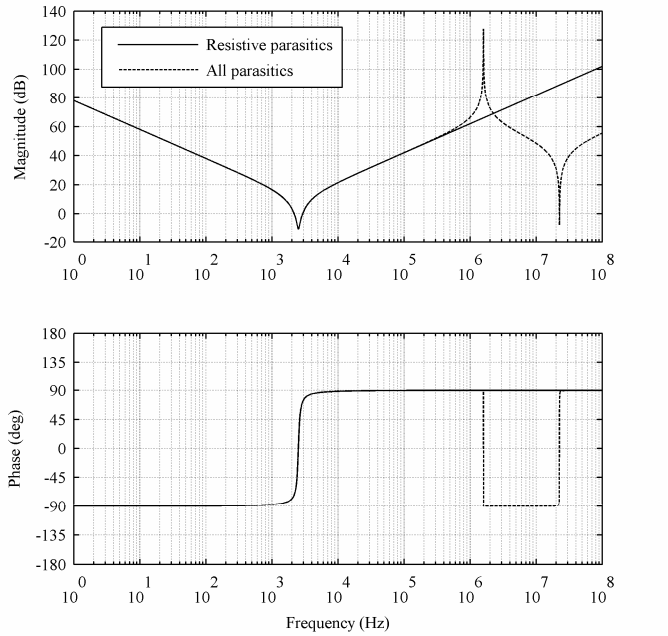


Figure 2.3. *EMI-filter input impedance with ideal voltage source and constant current load.*

The parasitic elements cause extra resonances at megahertz frequencies. The simulations were done in PSPICE to save time and the component values have no special meaning. The main inductance and capacitance was 200µH and 20µF and the parasitic inductance and capacitance was 1µH and 50pF, respectively. It has to be considered that the simulations at such high frequencies are not necessarily very accurate in practical designs. It is hard to predict all the small things like circuit board layout effective at the mega- and gigahertz frequencies. Radio frequency engineering expertise is required from the designer and/or the design software. Commercial EMI-filters designed for line connection are usually little more complicated containing e.g. additional common mode choke, but the main point that electric load input impedances might have harmful high frequency resonances is not changed. Resonances are caused by the cabling and diode rectifier voltage smoothing capacitors as well.

The EMI-filters are optimized to pass the existing emission standards as cost effectively as possible. The existing EMC standards are designed to protect analog radio communication and the standards does not consider the possibility of using power line communication technologies (PLC). The communication frequencies for AMR land between 9-95kHz and for internet connection between 1-30MHz [20]. The PLC uses voltage signals and any series resonance at communication frequency results to high currents causing attenuation of the communication signal by shunting. This has been reported as the most severe reason over emitted noise for failed communication in [21] with actual case example. High currents with the PLC and e.g. energy saving lamps and flat screen LCD televisions are measured to appear in [22].

2.3. Stability

The internal and input-output stability of an interconnected (cascaded) system is well-defined e.g. in [23]. The system shown in Figure 2.4 consists of two subsystems S and L and is defined by the input ($\hat{u}_{in1}$, $\hat{\imath}_{o2}$), output ($\hat{\imath}_{in1}$, $\hat{u}_{o2}$) and intermediate (z , $\bar{z}$) variables. For the stability to exist, all the transfer functions in the mappings from the input variables to the intermediate and output variables have to be stable.

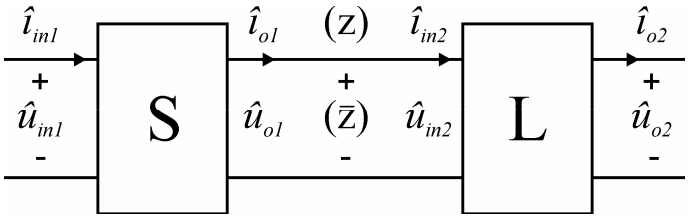


Figure 2.4. *The cascaded system.*

The subsystems can be represented in matrix form shown in (2.6) if the matrix entries are assumed to be scalars. The resulting mappings are as shown in (2.7) and (2.8).

$$\begin{bmatrix} \hat{\imath}_{in1} \\ \bar{z} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} \hat{u}_{in1} \\ z \end{bmatrix}$$
$$\begin{bmatrix} z \\ \hat{u}_{o2} \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \begin{bmatrix} \bar{z} \\ \hat{\imath}_{o2} \end{bmatrix} \tag{2.6}$$

$$\begin{bmatrix} z \\ \bar{z} \end{bmatrix} = \begin{bmatrix} \dfrac{S_{21}L_{11}}{1-S_{22}L_{11}} & \dfrac{L_{12}}{1-S_{22}L_{11}} \\ \dfrac{S_{21}}{1-S_{22}L_{11}} & \dfrac{S_{22}L_{12}}{1-S_{22}L_{11}} \end{bmatrix} \begin{bmatrix} \hat{u}_{in1} \\ \hat{\imath}_{o2} \end{bmatrix} \tag{2.7}$$

$$\begin{bmatrix} \hat{\imath}_{in1} \\ \hat{u}_{o2} \end{bmatrix} = \begin{bmatrix} S_{11} + \dfrac{S_{12}S_{21}L_{11}}{1-S_{22}L_{11}} & \dfrac{S_{12}L_{12}}{1-S_{22}L_{11}} \\ \dfrac{S_{21}L_{21}}{1-S_{22}L_{11}} & L_{22} + \dfrac{S_{22}L_{12}L_{21}}{1-S_{22}L_{11}} \end{bmatrix} \begin{bmatrix} \hat{u}_{in1} \\ \hat{\imath}_{o2} \end{bmatrix} \tag{2.8}$$

The internal and input-output stability depends on the stability of $1/(1-S_{22}L_{11})$ if the original transfer functions S_{ij} and L_{ij} are stable (i.e. have finite magnitudes). The transfer functions $S_{22} = -Z_{o\text{-}S}$ and $L_{11} = Y_{in\text{-}L}$ form the impedance ratio $Z_{o\text{-}S}/Z_{in\text{-}L}$ also known as minor-loop gain [6]. According to Nyquist stability criterion, the instability occurs when $Z_{o\text{-}S} = -Z_{in\text{-}L}$ (i.e. $|Z_{o-S}| = |Z_{in-L}|$ and $\angle Z_{o-S} = \angle Z_{in-L} - 180°$) even if the subsystems are stable in stand-alone operation. This impedance-ratio-based stability criterion is widely cited in the literature and used to define safe load and source profiles. This makes the

evaluating of the impedances important for stability analysis. The problem is how to analytically define or measure the input and output impedances of a converter with sinusoidal input and/or output. The DC-DC modeling is a relatively known issue.

2.4. Input Impedance

A DC-DC converter can be assumed to operate with constant input and output such that the steady-state operating point may be identified and small-signal linearization technique can be applied to the nonlinear averaged model and the converter characteristics can be solved analytically [24]. In case of an AC-DC converter, such as the PFC converter, the sinusoidal input is time-varying and direct linearization is not possible [25]. Four different linearization methods are discussed in [26] to be used with time-varying nonlinear systems:

A) *Phasor analysis:* The sinusoidal input voltage and current are treated as phasors which amplitude and phase angle are time-varying and hence can be treated as dynamic variables. Since the phasors are constant in the steady-state operation point the conventional small-signal linearization may be applied. One limitation is that phasor-based models are valid only below fundamental frequency. Another limitation is that small-signal impedance cannot be obtained [26].
B) *DQ reference frame modeling:* The rotating reference frames are usually used in the control systems of three-phase variable-speed motor drives and space-vector-modulated rectifiers and inverters. When the sinusoidal line variables are transformed into the reference frame rotating at the line frequency, the AC variables become DC variables. Now the small-signal analysis is applicable. The method may be used only with three-phase systems.
C) *Reduced-order modeling:* The reduced order modeling is based on constant DC-link capacitor voltage assumption. This eliminates nonlinearity of the model but is applicable only at high frequencies where the assumption is justified. This method is used with the PFC in [27].
D) *Harmonic linearization:* With harmonic linearization the small-signal linear models are developed by linearizing the time-varying systems along the periodic operation trajectories (single or multiple sinusoidal components). Responses to small harmonic perturbation at a system variable are determined from the other variables of interest to extract corresponding components at the perturbation frequency. The method is used with the PFC in [25].

In [28] a method called double averaging was used to model PFC converters. After the usual averaging over the switching frequency, the model is subsequently averaged over one line period to get rid of the time-varying input. Again the conventional linearization technique may be applied. Such impedance model predicts the input current response to perturbation at the input voltage amplitude [29] (i.e. from input voltage envelope to

input current envelope), which does not apply to the definition of the input impedance and thus according to [25] cannot be used in the stability analysis of an interconnected system.

A low frequency input impedance model is built in [25] using harmonic linearization. This model predicts resistive impedance at low frequencies. With resistive input the PFC converter source-load stability problems would be highly improbable, still low frequency oscillation is measured with the PFC supplied by ferroresonant transformer or UPS (uninterruptable power supply) in [29]. In [30], oscillation is measured with engine generator. The instability is associated with the negative incremental resistance, which is shown at the low frequencies in the envelope impedance as simulated and measured later in this thesis. Even if the envelope impedance really would not have anything to do with source-load stability analysis as claimed, it is interesting anyway since it gives information of load behavior during the changes in the input voltage amplitude, e.g. during the voltage dips.

The magnitude of the load input impedance (i.e. input resistance) is given by the ratio of small-signal changes in input voltage over the small-signal changes in input current. The value of the negative resistance depends on the converter operating point and hence is a dynamic variable.

$$R_{in} \approx \frac{\Delta u_{in}}{\Delta i_{in}} \tag{2.9}$$

For constant power load a positive change in the input voltage results to a negative change in the input current and vice versa. The negative input resistance can be calculated assuming that constant input power is proportional to the output power and efficiency ($P = P_{out} / \eta = P_{in} = u_{in} i_{in}$) and differentiating the voltage with respect to the current.

$$\frac{du_{in}}{di_{in}} = -i_{in}^{-2} P_{in} = -\left|\frac{P_{in}}{i_{in}^2}\right| = -\left|\frac{u_{in}^2}{P_{in}}\right| = -\left|\frac{u_{in}}{i_{in}}\right| = -R_{in} \tag{2.10}$$

Negative input resistance reduces the damping of the system and exposes it to oscillations [7, 31]. The negative input resistance can be seen as -180˚ phase in the DC input impedance at the low frequencies where the power can be maintained constant (despite the changes in the input voltage) by the control system of the load converter. Even if some of the existing methods to model single-phase AC systems does not support the existence of negative resistance, its existence can be observed from the amplitude modulation response in frequency domain or from the input voltage transient responses in time domain.

3. DYNAMICS OF REGULATED CONVERTERS

The open-loop dynamics of a voltage-mode-controlled converter is typically presented as a set of transfer functions known as the G-parameter set shown in (3.1). The meaning of the transfer functions can be concluded by means of the output vector $\left[\hat{\imath}_{in} \quad \hat{u}_o\right]^T$ and input vector $\left[\hat{u}_{in} \quad \hat{\imath}_o \quad \hat{c}\right]^T$, where $\hat{c}$ stands for the general control variable. The transfer functions in (3.1) represent only the internal dynamics of the converter, i.e. the effects of the load and the source are removed which is advantageous since the load and source are not generally known. Such transfer functions are known as unterminated transfer functions and can be derived or measured by using an ideal voltage source and ideal constant-current load. The G-parameter set is presented as a circuit theoretical two-port model in Figure 3.1 [23].

$$\begin{bmatrix} \hat{\imath}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y_{in-o} & T_{oi-o} & G_{ci} \\ G_{io-o} & -Z_{o-o} & G_{co} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{\imath}_o \\ \hat{c} \end{bmatrix} \tag{3.1}$$

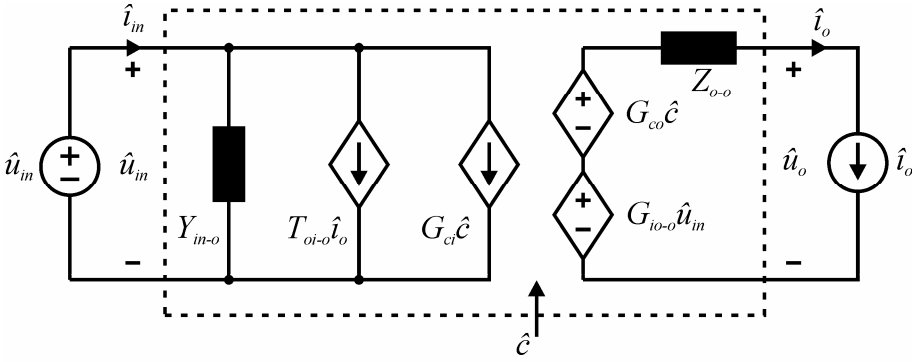


Figure 3.1. *The two-port model with ideal source and load.*

At the presence of a non-ideal source and load, the two-port model is shown in Figure 3.2, where the input port is Norton's equivalent circuit and the output port Thevenin's equivalent circuit, where $Y_N = Y_{in\text{-}o}$, $\hat{\imath}_N = T_{oi\text{-}o}\hat{\imath}_o + G_{ci}\hat{c}$, $Z_T = Z_{o\text{-}o}$ and $\hat{u}_T = G_{io\text{-}o}\hat{u}_{in} + G_{co}\hat{c}$, respectively.

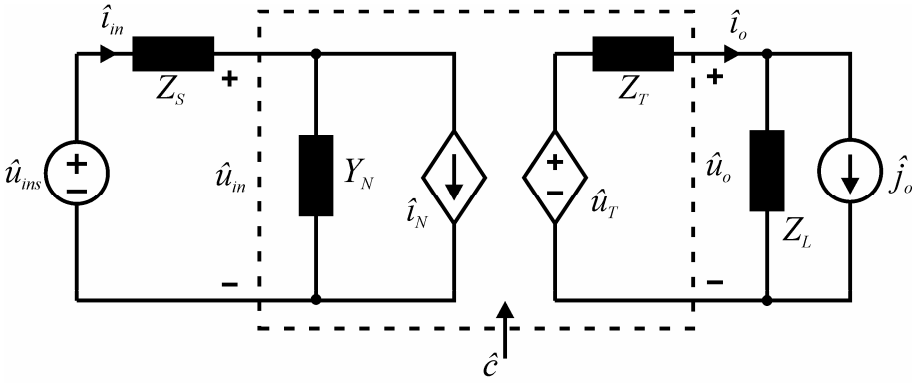


Figure 3.2. *Two-port model with non-ideal source and load.*

The effect of load impedance Z_L on converter dynamics can be found by solving $\hat{\imath}_o$ from Figure 3.2 yielding (3.2). The source impedance Z_S effect can be found by solving $\hat{u}_{in}$ yielding (3.3). Substituting the solved $\hat{\imath}_o$ or $\hat{u}_{in}$ in (3.1) yields the load- and source-affected sets defined in (3.4) and (3.5), respectively [32].

$$\hat{\imath}_o = \frac{G_{io-o}\hat{u}_{in} + G_{co}\hat{c} + Z_L\hat{j}_o}{Z_L + Z_{o-o}} \tag{3.2}$$

$$\hat{u}_{in} = \frac{\hat{u}_{ins} - Z_S T_{oi-o}\hat{\imath}_o - Z_s G_{ci}\hat{c}}{1 + Z_S Y_{in-o}} \tag{3.3}$$

$$\begin{bmatrix} \hat{\imath}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y_{in-o} + \dfrac{G_{io-o}T_{oi-o}}{Z_L + Z_{o-o}} & \dfrac{Z_L T_{oi-o}}{Z_L + Z_{o-o}} & G_{ci} + \dfrac{G_{co}T_{oi-o}}{Z_L + Z_{o-o}} \\ \dfrac{G_{io-o}}{1 + \dfrac{Z_{o-o}}{Z_L}} & -\dfrac{Z_{o-o}}{1 + \dfrac{Z_{o-o}}{Z_L}} & \dfrac{G_{co}}{1 + \dfrac{Z_{o-o}}{Z_L}} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{j}_o \\ \hat{c} \end{bmatrix} \tag{3.4}$$

$$\begin{bmatrix} \hat{\imath}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} \dfrac{Y_{in-o}}{1 + Z_S Y_{in-o}} & \dfrac{T_{oi-o}}{1 + Z_S Y_{in-o}} & \dfrac{G_{ci}}{1 + Z_S Y_{in-o}} \\ \dfrac{G_{io-o}}{1 + Z_S Y_{in-o}} & -\dfrac{1 + Z_S Y_{in-sc}}{1 + Z_S Y_{in-o}} \cdot Z_{o-o} & \dfrac{1 + Z_S Y_{in-\infty}}{1 + Z_S Y_{in-o}} \cdot G_{co} \end{bmatrix} \begin{bmatrix} \hat{u}_{ins} \\ \hat{\imath}_o \\ \hat{c} \end{bmatrix} \tag{3.5}$$

Ideal input admittance $Y_{in-\infty}$ and short-circuit input admittance Y_{in-sc} in the source affected sets are defined in (3.6).

$$Y_{in-\infty} = Y_{in-o} - \frac{G_{io-o}G_{ci}}{G_{co}}$$
$$Y_{in-sc} = Y_{in-o} + \frac{G_{io-o}T_{oi-o}}{Z_{o-o}} \tag{3.6}$$

The non-ideal source and load can be seen to have effect on the dynamics of a converter. For detailed analysis of the matter References [23] and [32] are recommended. The presented G-parameters can be used to represent any voltage-input-voltage-output electrical system and used e.g. in control system design and stability analysis. Output dynamics of such switched mode converter is presented in Figure 3.3 as a control-block diagram.

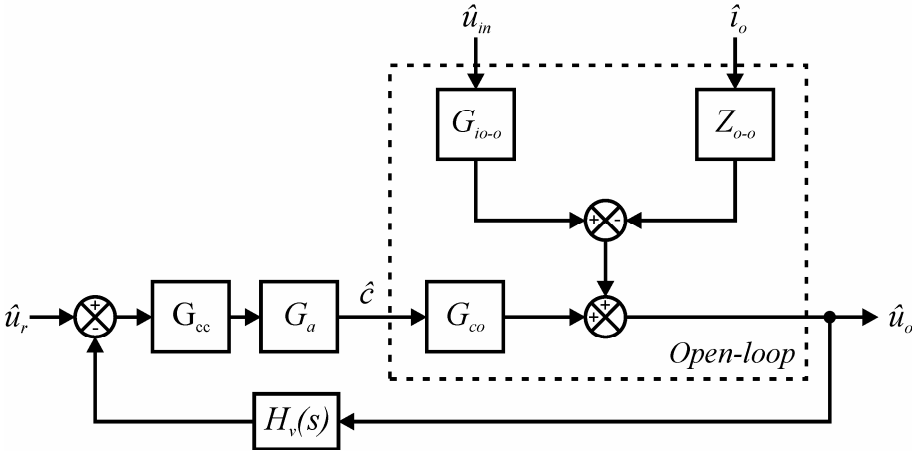


Figure 3.3. *Control-block diagram of a switched-mode converter output dynamics.*

According to Figure 3.3 the corresponding voltage loop gain can be presented as shown in (3.7) where $H_v(s)$ denotes the output-voltage sensing gain, G_{cc} the controller transfer function, G_a the modulator gain and G_{co} the control-to-output transfer function [23].

$$L(s) = H_v(s)G_{cc}G_aG_{co} \tag{3.7}$$

The stability margins of a converter can be extracted from the loop gain. In the next section, a popular method to obtain the G-parameters is introduced with a boost converter as an example. Then the state-space representation is generated also for an EMI filter and unstable cascaded system is designed in purpose of demonstrating the validity of the stability criterion introduced in Section 2.3.

3.1. State-Space Averaging

The famous state-space averaging technique in CCM (continuous conduction mode) [33] will be briefly presented in this chapter. The procedures involved in the state-space averaging for switching converter power stages are as follows. First the input, output and state variables are defined. Then the converter switch on-time and off-time equations for state and output variables have to be solved using Kirchhoff's current and voltage laws yielding the converter power stage presented in the state-space forms. The on-time equations multiplied with the duty ratio (*d*), and the off-time equations multiplied with the complement of the duty ratio (*d'=1-d*) are summed then together yielding the averaged state-space representation.

To obtain small-signal state space, a steady-state operation point has to be solved. A DC-DC converter can be assumed to operate with constant input and output and the steady-state operation point can be solved by letting the derivatives to be zero. The small-signal state space can now be solved from the averaged state space by linearizing the equations (i.e. developing the proper partial derivatives). The G-parameter set in Laplace-domain can be derived by matrix manipulation methods. The obtained models are valid up to half the switching frequency [34]. The G-parameter set for a boost converter power-stage in Figure 3.4 will be derived next.

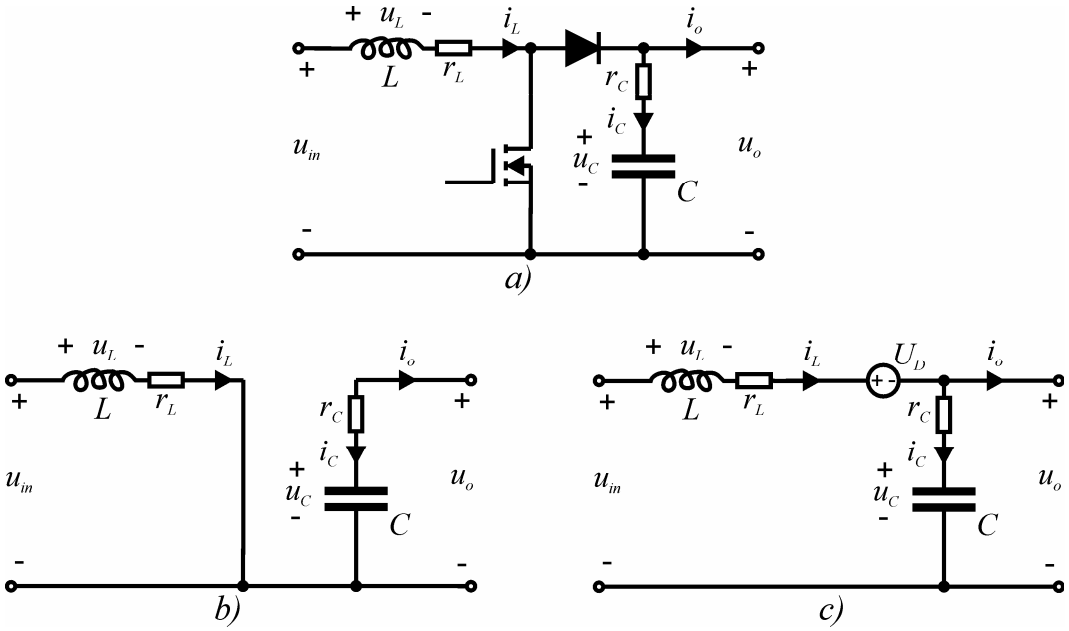


Figure 3.4. *a) Boost power stage and the switch b) on- and c) off-time subcircuits.*

The input, output and state variables will be defined first. The input variables are input voltage and output current. The output variables are input current and output voltage. The state variables are inductor current and capacitor voltage. Applying the Kirchhoff's current and voltage laws we get the on- and off-time equations (3.8) and (3.9), respectively. The voltage loss of the diode is assumed to be U_D.

$$\begin{aligned} u_L &= u_{in} - r_L i_L \\ i_C &= -i_o \\ u_o &= u_C + r_C i_C \\ i_{in} &= i_L \end{aligned} \tag{3.8}$$

$$\begin{aligned} u_L &= u_{in} - u_o - U_D - r_L i_L \\ i_C &= i_L - i_o \\ u_o &= u_C + r_C i_C \\ i_{in} &= i_L \end{aligned} \tag{3.9}$$

According to the basic circuit theory, the inductor-current and capacitor-voltage derivatives can be presented as $\frac{di_L}{dt} = \frac{u_L}{L}$, and $\frac{du_C}{dt} = \frac{i_C}{C}$, respectively, yielding the on- and off-time state-space equations as shown in (3.10) and (3.11).

$$\begin{aligned} \frac{di_L}{dt} &= -\frac{r_L i_L}{L} - \frac{u_{in}}{L} \\ \frac{du_C}{dt} &= -\frac{i_o}{C} \\ i_{in} &= i_L \\ u_o &= u_C - r_C i_o \end{aligned} \tag{3.10}$$

$$\begin{aligned} \frac{di_L}{dt} &= -\frac{(r_L + r_C) i_L}{L} - \frac{u_C}{L} + \frac{u_{in}}{L} + \frac{r_C i_o}{L} - \frac{U_D}{L} \\ \frac{du_C}{dt} &= \frac{i_L}{C} - \frac{i_o}{C} \\ i_{in} &= i_L \\ u_o &= r_C i_L + u_c - r_C i_o \end{aligned} \tag{3.11}$$

When the on-time equations are multiplied with *d* and off-time equations with *d'* (note that *d+d'=1*) and summed together, we get (3.12).

$$\begin{aligned} \frac{di_L}{dt} &= -\frac{\left(r_L + d' r_C\right) i_L}{L} - \frac{d' u_C}{L} + \frac{u_{in}}{L} + \frac{d' r_C i_o}{L} - \frac{d' U_D}{L} \\ \frac{du_C}{dt} &= \frac{d' i_L}{C} - \frac{i_o}{C} \\ i_{in} &= i_L \\ u_o &= d' r_C i_L + u_C - r_C i_o \end{aligned} \tag{3.12}$$

By developing the proper partial derivatives from (3.12) we get the linearized small-signal state-space representation in (3.13). The *hat* over the variables means small perturbation around the corresponding steady-state value.

$$\begin{aligned}
\frac{d\hat{i}_L}{dt} &= -\frac{\left(r_L + D'r_C\right)\hat{i}_L}{L} - \frac{D'\hat{u}_C}{L} + \frac{\hat{u}_{in}}{L} + \frac{D'r_C\hat{i}_o}{L} + \frac{U_o + U_D + r_C\left(I_L - I_o\right)}{L}\hat{d} \\
\frac{d\hat{u}_C}{dt} &= \frac{D'\hat{i}_L}{C} - \frac{\hat{i}_o}{C} - \frac{I_L\hat{d}}{C} \\
i_{in} &= \hat{i}_L \\
\hat{u}_o &= \hat{u}_C + r_C C\frac{d\hat{u}_C}{dt}
\end{aligned} \tag{3.13}$$

When we denote that $x(t) = \begin{bmatrix} i_L & u_C \end{bmatrix}^T$, u(t)=$\begin{bmatrix} \hat{u}_{in} & \hat{i}_o & \hat{d} \end{bmatrix}^T$, y(t)=$\begin{bmatrix} i_{in} & u_o \end{bmatrix}^T$, the small-signal state-space can be presented in matrix form as in (3.14).

$$\begin{aligned}
\frac{d\mathbf{x(t)}}{dt} &= \begin{bmatrix} -\frac{r_L + D'r_C}{L} & -\frac{D'}{L} \\ \frac{D'}{C} & 0 \end{bmatrix}\mathbf{x(t)} + \begin{bmatrix} \frac{1}{L} & \frac{D'r_C}{L} & \frac{Uo + U_D + r_C\left(I_L - I_o\right)}{L} \\ 0 & -\frac{1}{C} & -\frac{I_L}{C} \end{bmatrix}\mathbf{u(t)} \\
\mathbf{y(t)} &= \begin{bmatrix} 1 & 0 \\ 1 & r_C C\frac{d}{dt} \end{bmatrix}\mathbf{x(t)} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\mathbf{u(t)}
\end{aligned} \tag{3.14}$$

To solve the steady-state operating point from (3.13), we let the derivatives to be zero and the total values are replaced with the corresponding steady-state values. The resulting equations are shown in (3.15).

$$\begin{aligned}
&-\left(r_L + D'r_C\right)I_L - D'U_C + U_{in} + D'r_C I_o - D'U_D = 0 \\
&D'I_L - I_o = 0 \\
&I_{in} = I_L \\
&U_o = U_C
\end{aligned} \tag{3.15}$$

According to (3.15), we get (3.16) for the operating point from which the needed unknown numerical values can be solved to obtain the transfer functions for a practical converter.

$$\begin{aligned} U_o &= \frac{U_{in}}{D'} - U_D - \left(\frac{r_L}{D'^2} + \frac{Dr_C}{D'} \right) I_o \\ U_o &= U_C \\ I_L &= \frac{I_o}{D'} \\ I_{in} &= I_L \end{aligned} \tag{3.16}$$

The matrix equations in (3.14) can be presented as show in (3.17).

$$\begin{aligned} \frac{d\hat{\mathbf{x}}(\mathbf{t})}{dt} &= \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\hat{\mathbf{u}} \\ \hat{\mathbf{y}}(\mathbf{t}) &= \mathbf{C}\hat{\mathbf{x}} + \mathbf{D}\hat{\mathbf{u}} \end{aligned} \tag{3.17}$$

When converted to the corresponding frequency domain representation (the Laplace form), we get (3.18).

$$\begin{aligned} s\mathbf{X(s)} &= \mathbf{A} \cdot \mathbf{X(s)} + \mathbf{B} \cdot \mathbf{U(s)} \\ \mathbf{Y(s)} &= \mathbf{C} \cdot \mathbf{X(s)} + \mathbf{D} \cdot \mathbf{U(s)} \end{aligned} \tag{3.18}$$

Applying the matrix algebra the system may be solved as in (3.19).

$$\begin{aligned} \mathbf{X(s)} &= (s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} \cdot \mathbf{U(s)} \\ \mathbf{Y(s)} &= (\mathbf{C} \cdot (s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D}) \cdot \mathbf{U(s)} \end{aligned} \tag{3.19}$$

And finally we get the G-parameters from the system transfer function matrix $\mathbf{C} \cdot (s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D}$ as shown in (3.20) and (3.21) [34].

$$\begin{bmatrix} Y_{in-o} & T_{oi-o} \\ G_{io-o} & -Z_{o-o} \end{bmatrix} = \frac{\begin{bmatrix} \frac{s}{L} & \frac{D'(1+sr_CC)}{LC} \\ \frac{D'(1+sr_CC)}{LC} & -\frac{(r_L + DD'r_C + sL)(1+sr_CC)}{LC} \end{bmatrix}}{s^2 + s\frac{r_L + D'r_C}{L} + \frac{D'^2}{LC}} \tag{3.20}$$

$$\begin{bmatrix} G_{ci} \\ G_{co} \end{bmatrix} = \frac{\begin{bmatrix} \dfrac{\left(U_o + U_D + \dfrac{r_C D I_o}{D'}\right)Cs + I_o}{LC} \\ \dfrac{\left(D'(U_o + U_D) - \left(D' r_C + \dfrac{r_L}{D'}\right)I_o - s\dfrac{LI_o}{D'}\right)(1 + sr_C C)}{LC} \end{bmatrix}}{s^2 + s\dfrac{r_L + D' r_C}{L} + \dfrac{D'^2}{LC}} \tag{3.21}$$

Next a control system utilizing the VMC (voltage mode control) in CCM will be designed. In VMC, a control signal is compared to a PWM (pulse width modulation) ramp generating the duty ratio. Because the average inductor current lies exactly in the middle of the inductor current ripple band, the open loop transfer functions under VMC control are same as (3.20) and (3.21). With control modes like PCMC (peak current mode control) or ACMC (average current mode control) the duty ratio is not anymore independent but dynamically dependent on the control current and the other circuit elements and variables as well. The dynamical dependence is known as duty ratio constraints [35, 36]. A boost converter under VMC is shown in Figure 3.5. The converter parameters are defined in Table 3.1.

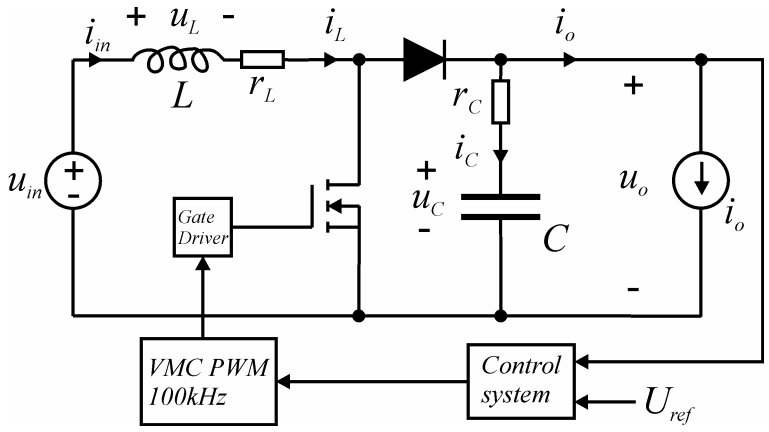


Figure 3.5. *Boost converter under voltage mode control.*

Table 3.1. *Boost converter parameters.*

u_{in}	u_o	i_o	L	r_L	C	r_C	U_D
20V	50V	2A	200μH	0.02Ω	470μF	0.05 Ω	0.7V

The steady-state value for the complement of the duty ratio can be expressed according to (3.16) as a quadratic equation shown in (3.22).

$$D'^2 - \frac{U_{in} - r_C I_o}{U_o + U_D - r_C I_o} D' + \frac{r_L I_o}{U_o + U_D - r_C I_o} = 0 \tag{3.22}$$

After defining the duty ratio, the control-to-output transfer function (G_{co}) can be solved numerically. The frequency response of G_{co} is shown in Figure 3.6.

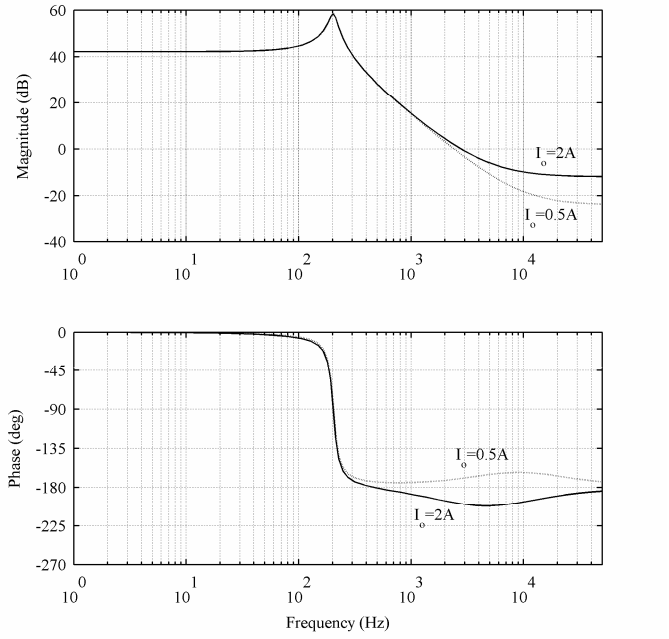


Figure 3.6. *Frequency responses of G_{co}.*

The practical control bandwidth is limited due to a right half plane (RHP) zero at 3066 Hz in the control-to-output transfer function. The limitation is most severe when the input voltage is at minimum and output power is at maximum since then the RHP zero is closest to the origin. The controller used is a PID-type (proportional-integral-derivative) controller shown in Laplace form in (3.23). The controller is designed to compensate the phase after the resonance to extend the control bandwidth (also known as loop-shaping technique). Following controller parameters was selected: $\omega_{z1}=2\pi*100Hz$, $\omega_{z2}=2\pi*200Hz$, $\omega_{p1}=2\pi*5kHz$, $\omega_{p2}=2\pi*50kHz$ and $K=70.8$. The controller frequency response is shown in Figure 3.7.

$$G_{cc}=\frac{K\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{s\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \tag{3.23}$$

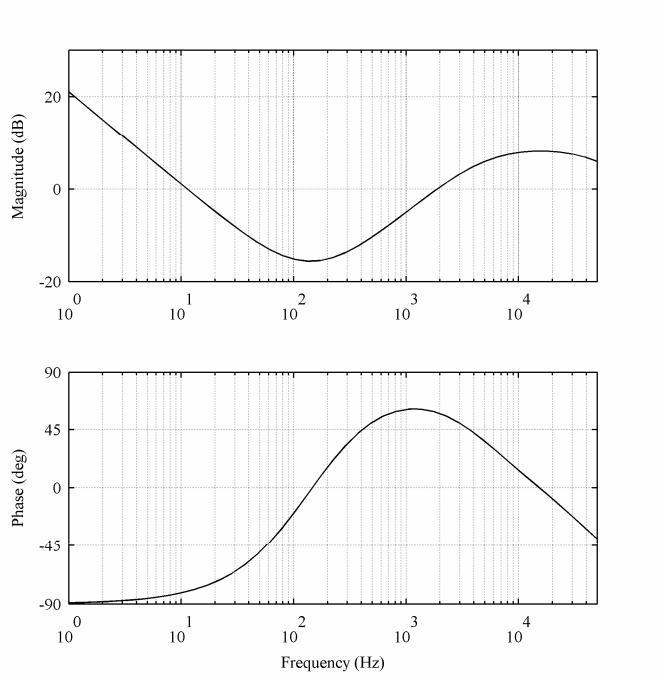


Figure 3.7. *Frequency response of G_{cc}.*

The resulting voltage loop gain is shown in Figure 3.8. The output voltage sensing gain is one and PWM ramp peak-to-peak voltage is 3V giving 1/3 for modulator gain. The phase margin (PM) is approximately 52˚ and the gain margin (GM) is approximately 11dB. Control bandwidth (CBW) is 1050Hz. The minimum margins are with the maximum power. As can be seen the margins are higher with 0.5A load current.

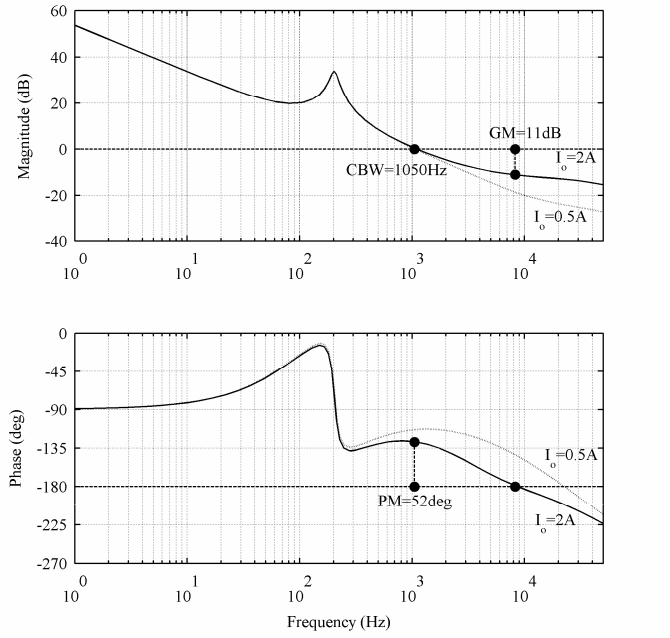
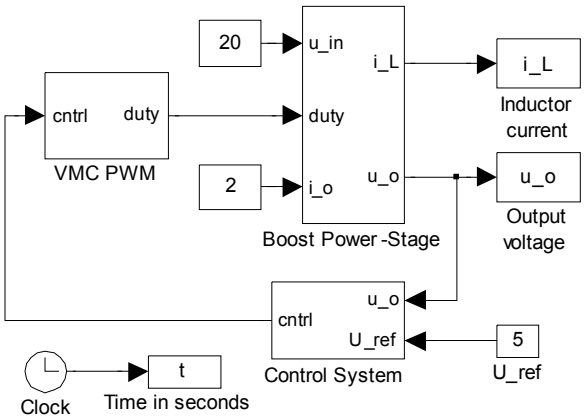
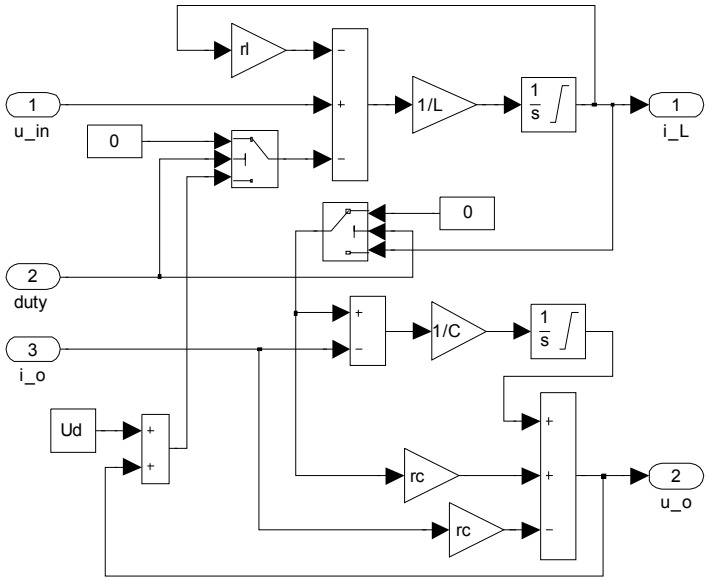


Figure 3.8. *The voltage loop gains.*

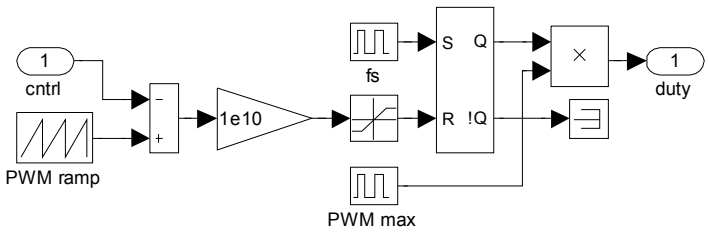
The boost converter is simulated in Matlab/Simulink. The Simulink model is shown in Figure 3.9. The power stage model can be built from (3.10) and (3.11).



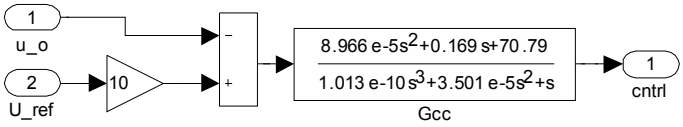
a) The overall model.



b) Boost power-stage.



c) VMC PWM.



d) Control system.

Figure 3.9. *The simulation setup for boost converter.*

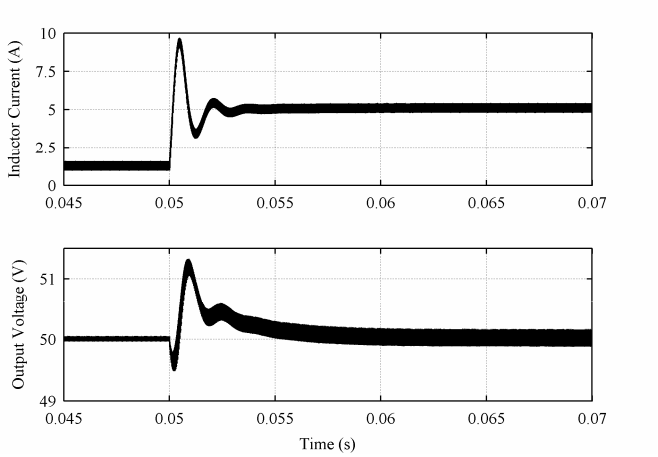


Figure 3.10. *Boost converter response to load step from 0.5A to 2A.*

The converter load current step response is shown in Figure 3.10. As can be seen the converter is stable and the response is quite fast, but due to overshoot (which could be analyzed from closed-loop output impedance) in the response, the design is not very good for a practical converter. However, the model is suitable for the simulations. In the next chapter, an input EMI-filter will be added to the model and the converter operation is checked again.

3.2. EMI-filter – Converter Example

A G-parameter transfer function set for an EMI-filter shown in Figure 3.11 will be built applying the same procedures as with the boost converter in Section 3.1. Due to the passive linear circuit, the modeling is quite simple and the transfer functions are briefly constructed. Naturally the control variable is now zero (i.e. it does not exist).

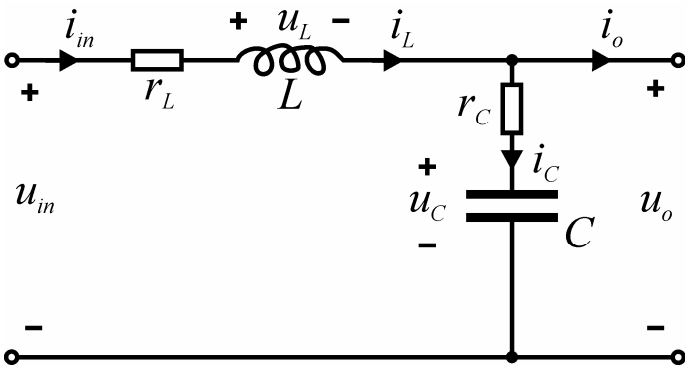


Figure 3.11. *LC-type EMI-filter with resistive parasitics.*

The state-space representation for the EMI-filter is shown in (3.24) and the matrix form in (3.25). The same input, output and state variables are used as with the boost converter.

$$\begin{aligned}
\frac{di_L}{dt} &= -\frac{(r_L + r_C)}{L} i_L - \frac{1}{L} u_C + \frac{1}{L} u_{in} + \frac{r_C}{L} i_o \\
\frac{du_C}{dt} &= \frac{1}{C} i_L - \frac{1}{C} i_o \\
u_o &= r_C i_L + u_C - r_C i_o \\
i_{in} &= i_L
\end{aligned} \tag{3.24}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{du_C}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_L + r_C}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ u_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{r_C}{L} \\ 0 & -\frac{1}{C} \end{bmatrix} \begin{bmatrix} u_{in} \\ i_o \end{bmatrix}$$

$$\begin{bmatrix} i_{in} \\ u_o \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ r_C & 1 \end{bmatrix} \begin{bmatrix} i_L \\ u_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & -r_C \end{bmatrix} \begin{bmatrix} u_{in} \\ i_o \end{bmatrix} \tag{3.25}$$

Due to the passive linear circuit, the corresponding small-signal representation is the same as (3.25) but the total values have to be replaced by means of the small signal values in the corresponding matrix vectors. The state-space in (3.25) has to be transformed into Laplace domain in order to obtain the system transfer functions. The Laplace representation is shown in (3.26) and the resulting system transfer function matrix ($\mathbf{G}(s) = \mathbf{C} \cdot (s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D}$) is shown in (3.27).

$$s\begin{bmatrix} I_L(s) \\ U_C(s) \end{bmatrix} = \begin{bmatrix} -\frac{r_L + r_C}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} I_L(s) \\ U_C(s) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{r_C}{L} \\ 0 & -\frac{1}{C} \end{bmatrix} \begin{bmatrix} U_{in}(s) \\ I_o(s) \end{bmatrix}$$

$$\begin{bmatrix} I_{in}(s) \\ U_o(s) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ r_C & 1 \end{bmatrix} \begin{bmatrix} I_L(s) \\ U_C(s) \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & -r_C \end{bmatrix} \begin{bmatrix} U_{in}(s) \\ I_o(s) \end{bmatrix} \tag{3.26}$$

$$\mathbf{G}(s) = \frac{\begin{bmatrix} \frac{s}{L} & \frac{1 + sr_C C}{LC} \\ \frac{1 + sr_C C}{LC} & -\frac{r_L(1 + s\frac{L}{r_L})(1 + sr_C C)}{LC} \end{bmatrix}}{s^2 + s\frac{r_L + r_C}{L} + \frac{1}{LC}} \tag{3.27}$$

The closed loop input admittance ($Y_{in\text{-}c}$) of the boost converter can be presented as shown in (3.28) [39]. The closed loop input impedance ($Z_{in\text{-}c}$) is naturally $1/Y_{in\text{-}c}$.

$$Y_{in-c} = Y_{in-o} - \frac{L(s)}{1+L(s)} \cdot \frac{G_{io-o} G_{ci}}{G_{co}} \tag{3.28}$$

Figure 3.12 shows the frequency responses of the converter closed loop input impedances at 0.5A and 2A load currents and the output impedance of the input EMI-filter with the parameters defined in Table 3.2.

Table 3.2. *EMI-filter parameters.*

L	C	r_L	r_C
500µH	1000µF	0.02Ω	0.06Ω

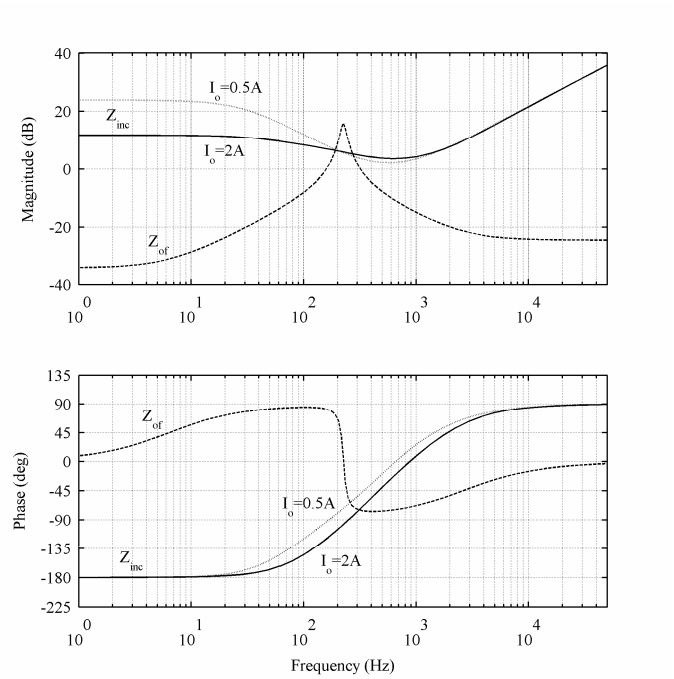


Figure 3.12. *Closed loop input impedances of the converter and output impedance of the EMI-filter.*

The stability can be easiest seen from the Nyquist plot. Briefly the Nyquist stability criterion for closed loop system is; if the plot does not encircle the point (-1, 0) in clockwise direction, the system is stable if the open loop transfer function is stable. According to Nyquist plots of $Z_{of}Y_{in\text{-}c}$ in Figure 3.13 the system is unstable with 2A load and stable with 0.5A load. As can be seen the phase of the input impedance does not have to be -180˚ to cause unstable operation with non-ideal source. The instability occurs when the phase difference of Z_{of} and $Z_{in\text{-}c}$ is 180˚ and the magnitude of the output impedance equals or is higher than the input impedance. Obviously the -180˚ phase of the load makes the system more prone to instability.

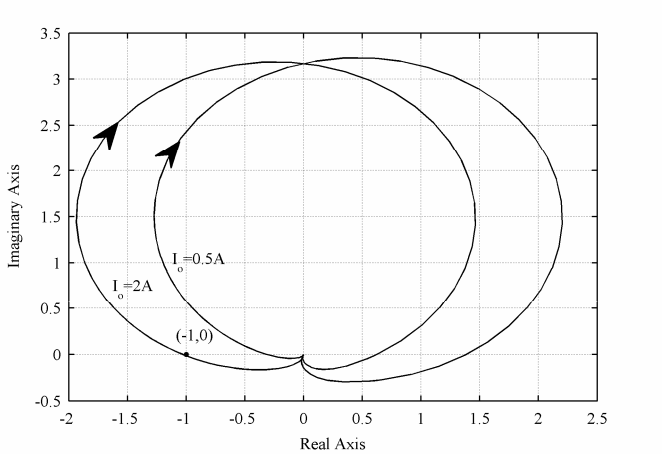


Figure 3.13. *Nyquist plots of $Z_{of}Y_{in\text{-}c}$.*

Behavior of the converter in stable and unstable conditions is shown in Figure 3.14. The load current is ramped from 0.5A to 2A during 10ms starting from *t=0.5s* and kept at 2A for 10ms. The load current is ramped back to 0.5A during 10ms starting from *t=0.52s*. As can be seen the performance is not very good even with 0.5A load but the system is stable unlike with 2A load current. The oscillation frequency is approximately 200Hz which is the resonant frequency of the EMI-filter. At 200Hz the magnitude plots of the associated impedances are equal and their phase difference is 180˚ at 2A load. The simulation setup is shown in Figure 3.15.

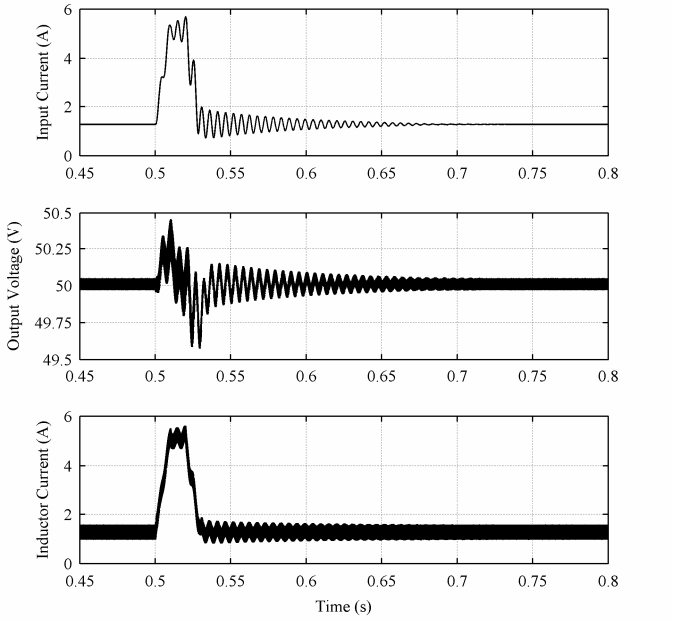
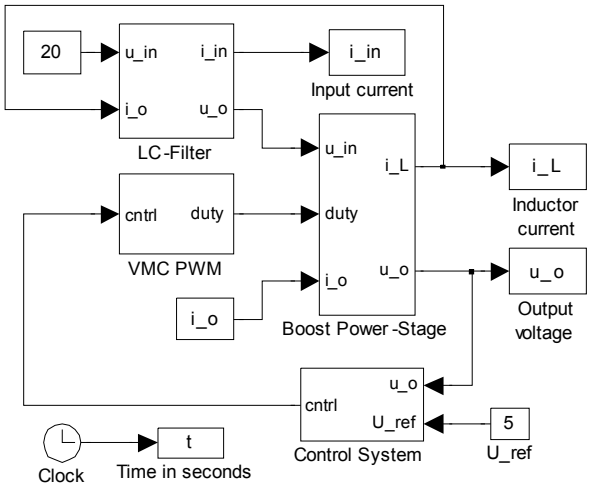
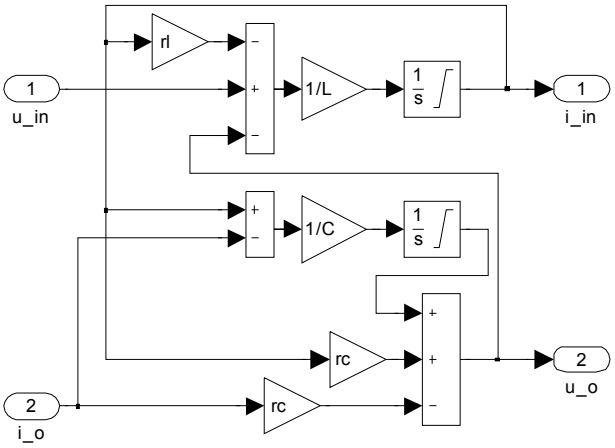


Figure 3.14. *Boost converter response to load change with input filter.*



a) The overall model.



b) LC-Filter.

Figure 3.15. *Simulation setup with input filter.*

The validity of the impedance-ratio based stability criterion was demonstrated in this chapter. In the next chapter, the boost-converter-based power factor corrector is designed. No analytical models will be built like in this chapter due to linearization problems with sinusoidal input, but the analysis is done based on simulations in time domain.

4. BOOST POWER FACTOR CORRECTOR

In order to meet harmonic distortion limits where needed, power factor correction must be used. The boost topology controlled with average current mode control (ACMC) operating in continuous conduction mode (CCM) is commonly used in PFC applications [37]. The ACMC is reviewed in [38]. For low power applications a boost converter operating at the boundary of CCM and DCM (discontinuous conduction mode) is also popular [39, 40]. Its main benefits compared to ACMC in CCM is that the reverse recovery losses of the boost diode are eliminated and the switch operates at zero-current turn-on, reducing turn-on losses. On the negative side the current stresses to components are higher and larger EMI-filter is needed at the input. Also the variable switching frequency may create problems [41].

4.1. Boundary Mode Control

Electronic ballasts for fluorescent lamps are common application using boundary mode operation [3]. Because electronic ballast is used in the measurements, the boundary mode operation is also discussed but the main simulations are done with the switching frequency averaged ACMC Simulink model. Control system for boundary mode PFC converter shown in Figure 4.1 is designed next.

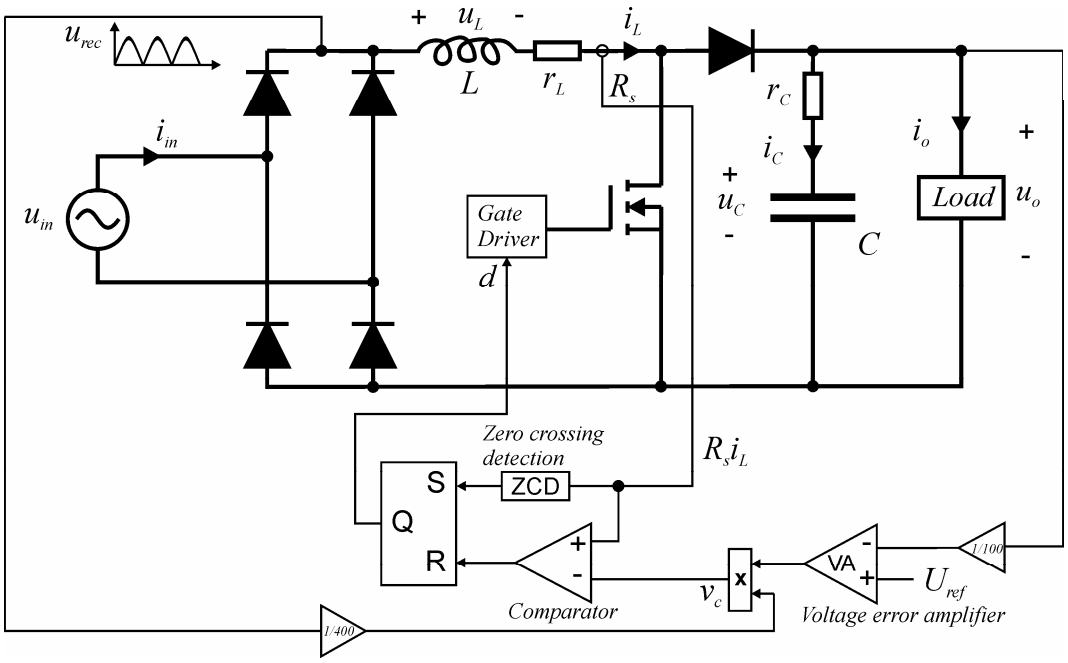


Figure 4.1. *Boost PFC converter operating in the boundary mode.*

The idea in PFC converters is to control the input current to follow the shape of the input voltage. With boost topology this can be done by controlling the inductor current to follow the full wave rectified input sine wave, which makes the use of boost topology convenient in PFC applications. The voltage error amplifier (VA) output is multiplied with the rectified input sine wave u_{rec} to generate the control signal v_c corresponding to the input voltage by shape. The control signal is used as a reference for the inductor current envelope. When the signal for inductor current ($R_s i_L$) reaches the value of v_c, the comparator resets the S-R latch (set-reset) and the switch is turned off. Turn-on signal is given by the zero crossing detection circuit when current reaches zero. The sinusoidal input current (average inductor current, Figure 4.2) results with a low-pass filtering of the converter input current (e.g. LC-filter, not shown in Figure 4.1).

The variable switching frequency depends on the inductor size, input voltage, output voltage and output power. Obviously the minimum frequency is at the peak of the input voltage, which can be seen in Figure 4.2, where the inductor current in boundary mode operation is shown. The switching frequency should always be higher than 20kHz (maximum audible frequency to humans) in order to avoid audible noise e.g. from the inductor. Also frequencies in the range of *30-40kHz* in light may disturb infrared applications [42].

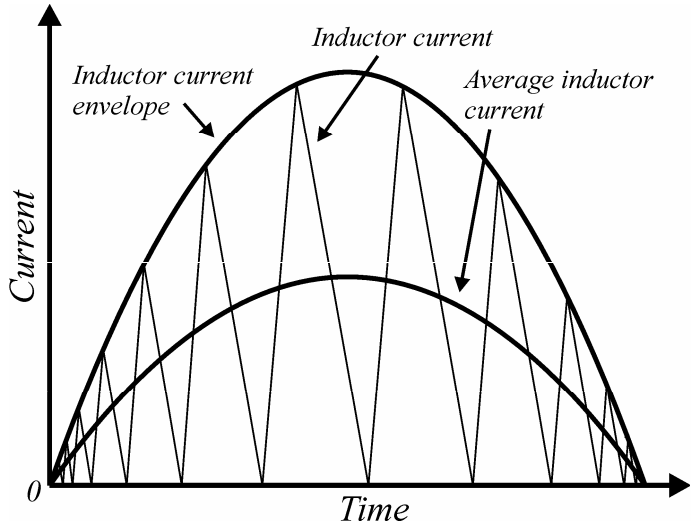


Figure 4.2. *Illustrated inductor current in boundary mode boost PFC.*

In ideal situation, the inductor current envelope is two times the average, and the peak value of inductor current may be solved as shown in (4.1).

$$I_{L,peak} = 2\sqrt{2}I_{in} = \frac{2\sqrt{2}P_o}{U_{in}} \tag{4.1}$$

Since the inductor current is in phase with the input voltage, the switch maximum on-time shown in (4.2) can be calculated from the inductor current peak value, inductance and peak input voltage.

$$t_{on,\max} = \frac{L}{\sqrt{2}U_{in}} I_{L,peak} = \frac{2LP_o}{U_{in}^2} \tag{4.2}$$

During the switch off-time, the inductor current down slope is defined by the difference of the output and input voltages. The maximum off-time is calculated in (4.3). The minimum switching frequency shown in (4.4) can now be derived since $T_{s,\max} = t_{on,\max} + t_{off,\max}$ and $f_{s,\min} = 1/T_{s,\max}$.

$$t_{off,\max} = \frac{2\sqrt{2}LI_{in}}{U_o - \sqrt{2}U_{in}} \tag{4.3}$$

$$f_{s,\min} = \frac{U_{in}\left(U_o - \sqrt{2}U_{in}\right)}{2LU_oI_{in}} = \frac{U_{in}^2\left(U_o - \sqrt{2}U_{in}\right)}{2LU_oP_o} \tag{4.4}$$

The minimum switching frequency is selected to be approximately 50kHz, which gives an inductor value of 0.5mH. The same basic parameters shown in Table 4.1 are used with every model.

Table 4.1. *Parameters for the boost PFC.*

u_{in}	R_s	L	U_D	r_L	r_C	C	P_{Load}
230V	1Ω	0.5mH	0.7V	100mΩ	200mΩ	470µF	190W

The voltage error amplifier must be slow enough not to distort the control signal with the 100Hz ripple at the output voltage. Ideally the output of the voltage error amplifier would not change during half the line cycle. The slower the controller is the more sinusoidal is the input current but transient behavior deteriorates. Due to lack of linearized analytical model, voltage loop gain has to be simulated by summing a small perturbation signal to the output voltage measurement. The loop gain can then be extracted by calculating the effect of the perturbation to the output voltage at corresponding frequency with FFT (fast Fourier transform).

A good practice to design the loop gain is to select reasonable values for the poles and zeros of the voltage error amplifier and its crossover frequency. From the first loop gain, it can be concluded how much the gain can be increased to reach desired stability margins or control bandwidth. The loop gains and the voltage error amplifier parameters will be shown in the simulation results for all the models.

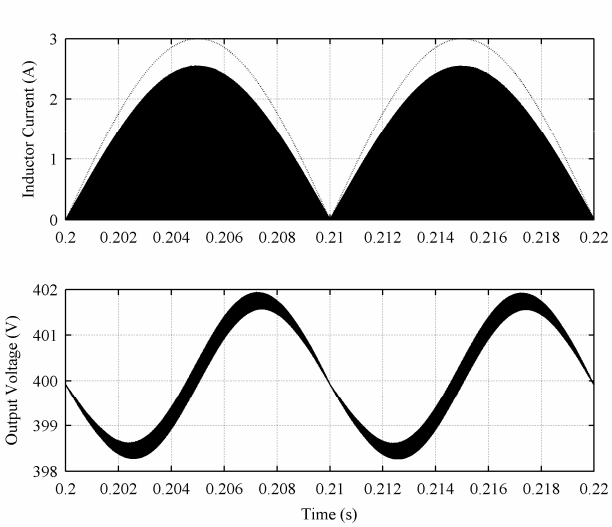


Figure 4.3. *Steady-state waveforms for boundary mode operation.*

Figure 4.3 presents the inductor current and output voltage steady-state waveforms. The output voltage reference is 400V. The dotted line represents the shape of the input voltage absolute value u_{rec}. The waveforms are as expected and the output voltage contains ripple at twice the line frequency, which may distort the input current if the voltage error amplifier is not designed properly.

4.2. Fixed Frequency ACMC

Fixed frequency ACMC boost converter popular in the PFC applications is discussed in this section. The main differences to the boundary mode can be seen from Figure 4.4.

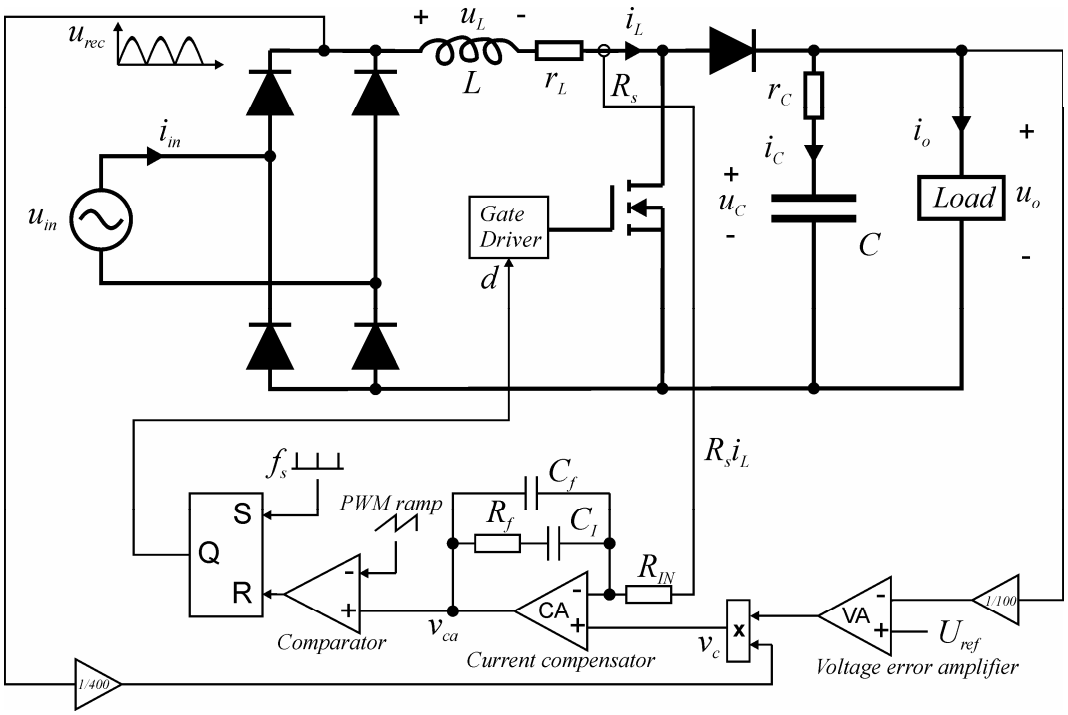


Figure 4.4. *Boost PFC converter with fixed frequency ACMC.*

Again the output of the voltage error amplifier is multiplied with the rectified input u_{rec} to create the control signal v_c shaped according to the input voltage. Then the control signal and the signal representing inductor current ($R_s i_L$) are passed through the PI-type current compensator and compared to the PWM ramp signal to generate the duty ratio [38]. The current compensator transfer function in Laplace form is shown in (4.5).

$$G_{ca} = \frac{K_f \omega_z \left(1 + \frac{s}{\omega_z}\right)}{s\left(1 + \frac{s}{\omega_p}\right)} \tag{4.5}$$

The angular frequencies ω_z (zero) and ω_p (pole) and the gain K_f are defined in (4.6).

$$\omega_z = \frac{1}{R_f C_I},\ \omega_p = \frac{C_f + C_I}{R_f C_f C_I},\ K_f = \frac{R_f C_I}{R_{IN}\left(C_f + C_I\right)} \tag{4.6}$$

According to Figure 4.4, the output of the current compensator can be calculated as shown in (4.7).

$$v_{ca} = \left(1 + G_{ca}\right) v_c - G_{ca} R_s i_L \tag{4.7}$$

The current compensator is designed fast to track the reference tightly. The switching frequency is selected to be 400kHz. The zero is placed at 10kHz to get high enough low frequency gain. K_f is set to 0dB and the pole is placed at 40kHz to filter switching frequency ripple from v_{ca}. The frequency response of G_{ca} is shown in Figure 4.5.

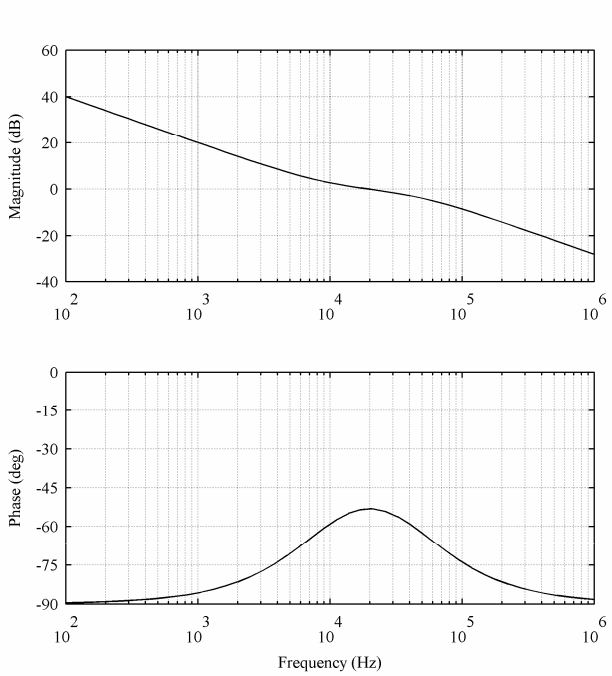


Figure 4.5. *Frequency response of G_{ca} when $\omega_z = 2\pi*10$ krad/s, $\omega_p = 2\pi*40$ krad/s and $K_f = 0$dB.*

The voltage error amplifier parameters and the loop gain are presented in simulation results. Figure 4.6 shows the steady state waveforms for the ACMC operation.

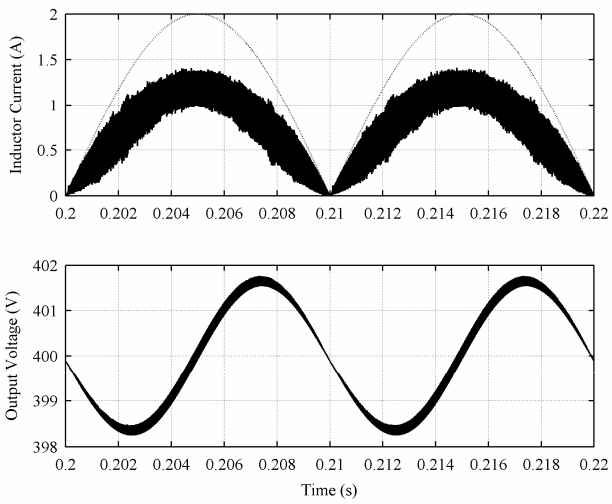


Figure 4.6. *Steady-state waveforms for ACMC operation.*

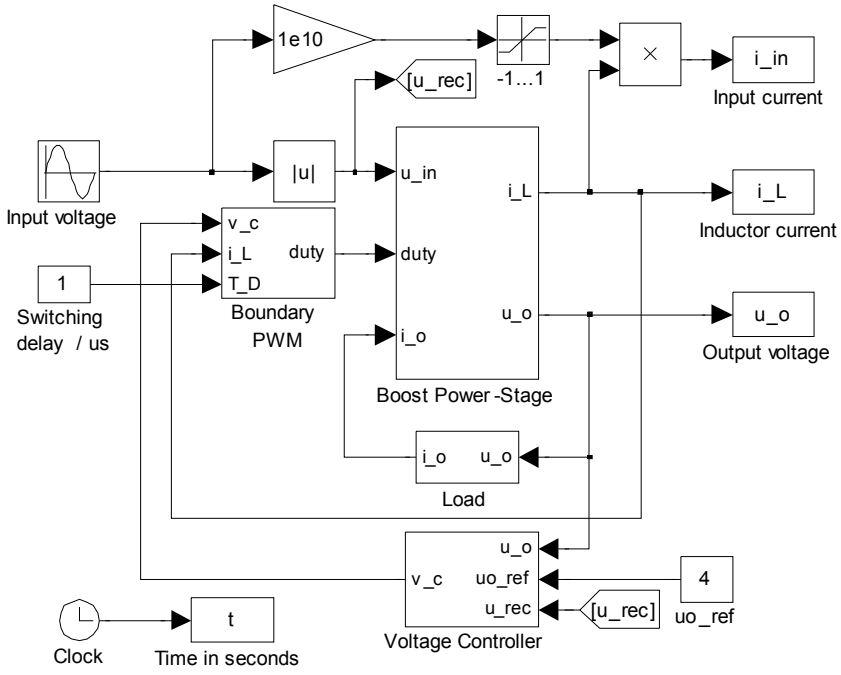
The dotted line represents the shape of u_{rec}. The main difference to the boundary mode operation is that the ripple components are clearly reduced and smaller components can be used in the input filter. The average inductor current is still the same.

4.3. Simulink Models

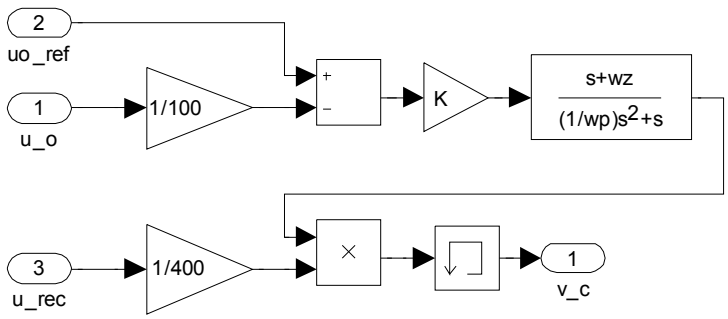
A boost DC-DC converter was modeled already in Section 3.1. The constructed Simulink model for boost power stage (Figure 3.9) can be used in the simulation models for the power factor correctors. The control signal has to be shaped according to the sinusoidal input and corresponding modulators are needed.

4.3.1. Boundary Mode

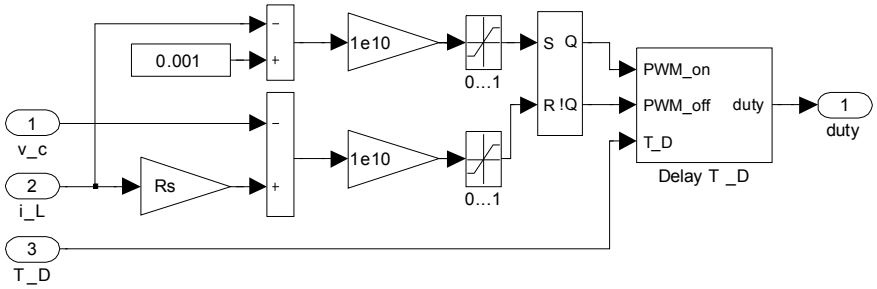
Simulation model for the boundary mode is presented in Figure 4.9. The output voltage reference is 400V and the input current can be calculated by multiplying the inductor current with the sign of the input voltage. The switching is delayed by 1µs to include small natural delay existing in practical applications. The control signal v_c for the inductor current is created in the voltage controller block. Also the PI-type voltage error amplifier is located in this block.



a) The overall model.



b) Voltage controller.



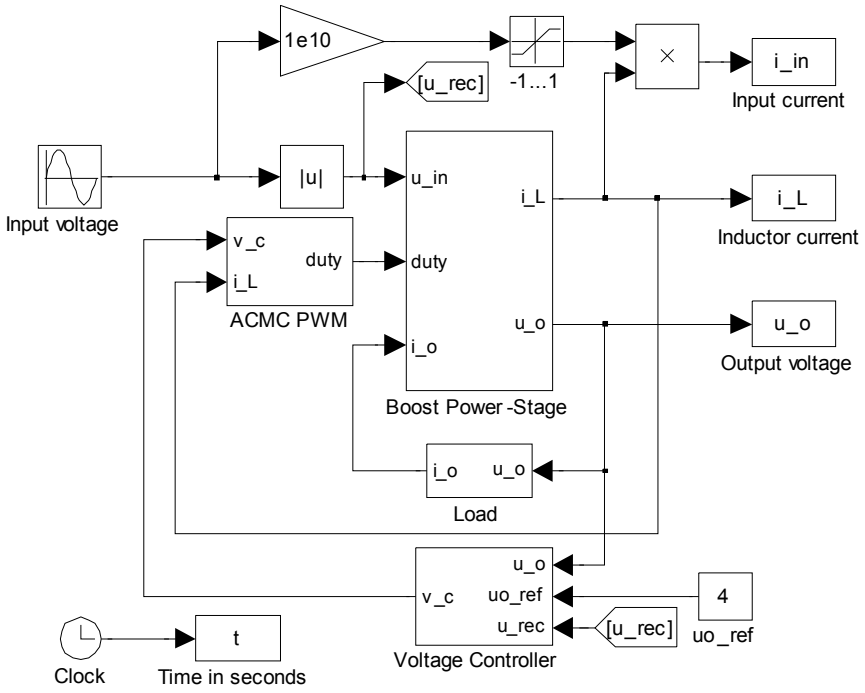
c) Boundary mode PWM.

Figure 4.7. *Simulation setup for boundary mode boost PFC.*

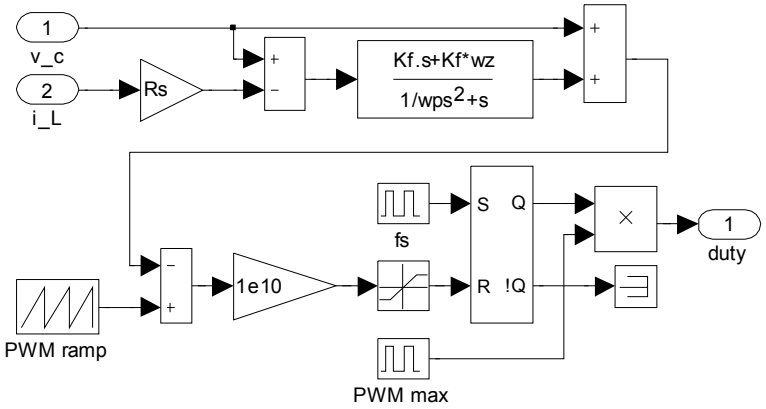
The high gain blocks and saturations in the PWM block shown in Figure 4.7 are used to represent Boolean type signals to show if the sums are positive, i.e. used to model the comparator.

4.3.2. ACMC

Fixed frequency ACMC simulation model is presented in Figure 4.8. Actually the only difference to boundary mode is in the modulator block, which also contains the current compensator.



a) The overall model.



b) ACMC PWM.

Figure 4.8. *Simulation setup for ACMC boost PFC.*

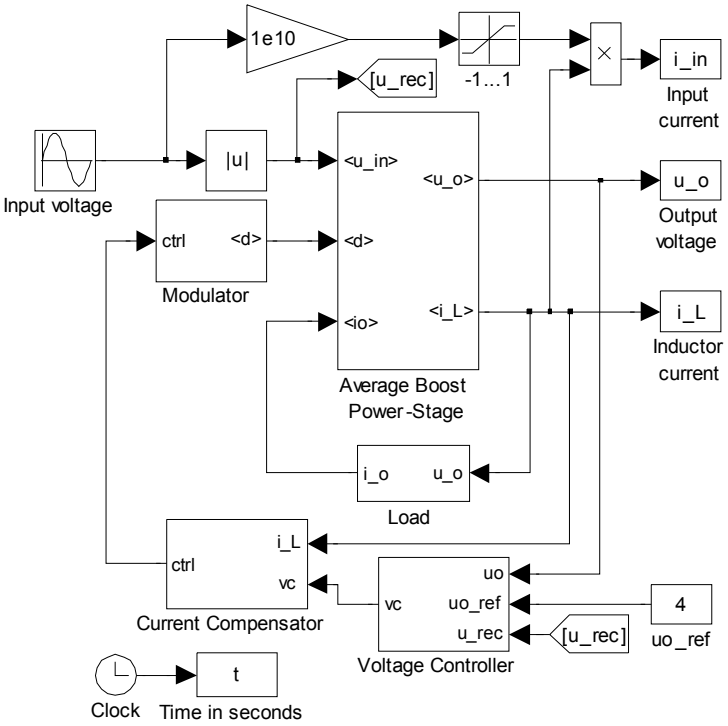
The current compensator output is compared to a PWM ramp similarly to voltage-mode-control to turn the switch off. The switch is turned on at constant frequency f_s. The maximum duty ratio can be limited.

4.3.3. Average ACMC

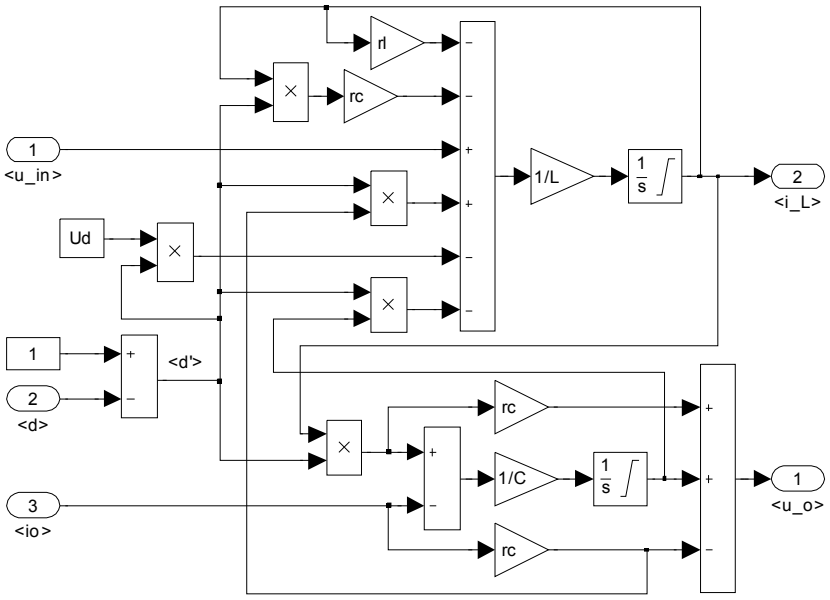
Average, or large signal, models instead of switching models for power factor correctors are often used to simplify simulations [37, 43]. Due to high frequency switching elements the computation times to obtain the simulation waveforms are long and the use of switching models may become impractical. The basic characteristics of a converter are not changed with average model so one is built for the ACMC PFC converter to ease the study. When the boost on-time (3.10) and off-time (3.11) equations are multiplied with the duty ratio d and the complement of the duty ratio d' (*1-d*), respectively, and summed together, we get averaged equations for the converter power stage as shown in (4.8). The variables in brackets are averaged over one switching cycle. The equations are not valid in DCM due to third, non-conducting, subcycle during the switching period.

$$\begin{aligned}
&\frac{d<i_L>}{dt}=\frac{-\left(r_L+<d'>r_C\right)<i_L>}{L}-\frac{<d'><u_C>}{L}+\frac{<u_{in}>}{L}\\
&+\frac{<d'>r_C<i_o>}{L}-\frac{<d'>U_D}{L}\\
&\frac{d<u_C>}{dt}=\frac{<d'><i_L>}{C}-\frac{<i_o>}{C}\\
&<i_{in}>=<i_L>\\
&<u_o>=<d'>r_C<i_L>+<u_C>-r_C<i_o>
\end{aligned} \tag{4.8}$$

The resulting switching cycle averaged model for ACMC boost PFC is shown in Figure 4.9. The averaged boost power stage model is based on (4.8). The switching elements have been replaced with the multiplying elements. Current compensator and voltage controller are the same as with the switching ACMC model. The modulator can be modeled as a constant gain [37].



a) The overall model.



b) Average boost power-stage.

Figure 4.9. *Simulation setup for average ACMC boost PFC.*

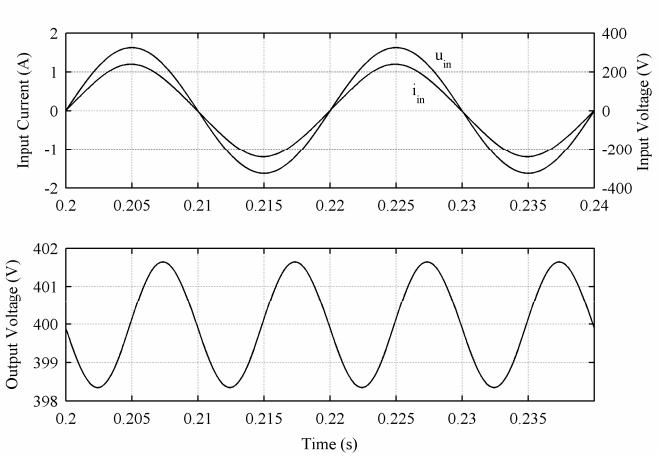


Figure 4.10. *Steady state operation of the average model.*

It can be seen from Figure 4.10 that the average model gives average values without switching frequency ripple for simulated waveforms. The absence of switching elements reduces computation time drastically. In the forthcoming time- and frequency domain simulations this average model is used if not otherwise stated.

4.4. Simulation Results

The voltage error amplifier is the same type as the current compensator in (4.5). The zero was placed at 5Hz, the pole frequency was selected to be 20Hz and the boost gain was set to 26dB to reach approximately 25Hz loop gain crossover frequency. The control bandwidth has to be small enough to achieve sinusoidal input current. The loop gains simulated with the average model is shown Figure 4.11. The loop gains were not simulated for the switching models.

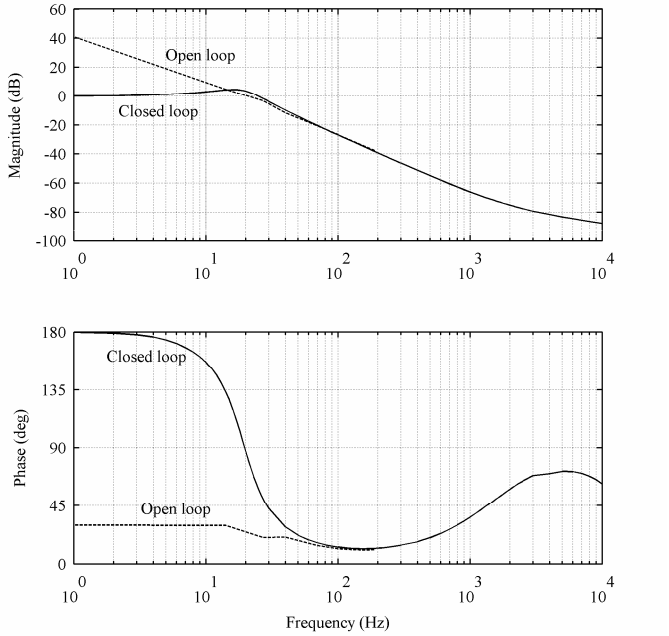


Figure 4.11. *Loop gains for the PFC.*

Input voltage feedforward (IVFF) control is a common method to improve transient behavior. In input voltage feedforward, the input voltage is low-pass filtered to create a signal representing the input voltage RMS-value. Then the control signal v_c is divided with square of that value to raise control signal gain when input voltage drops (or opposite if voltage raises). This also helps utilizing wide range of input voltages [44]. Differences in transient responses with the control systems are shown in Figure 4.12.

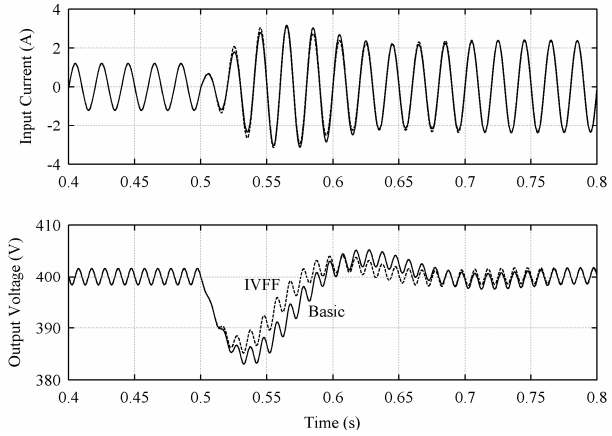


Figure 4.12. *Transient responses when input voltage is dropped to half.*

According to the transient responses in Figure 4.12, negative-incremental-resistance characteristics is obvious: When input voltage is dropped to half (from $230V_{RMS}$ to $115V_{RMS}$ at $t=0.5s$), the input current rises to twice the original. Although the current and voltage are in phase, the input impedance can not be resistive. Control system without feedforward is used in the frequency response simulations shown in Figure 4.13.

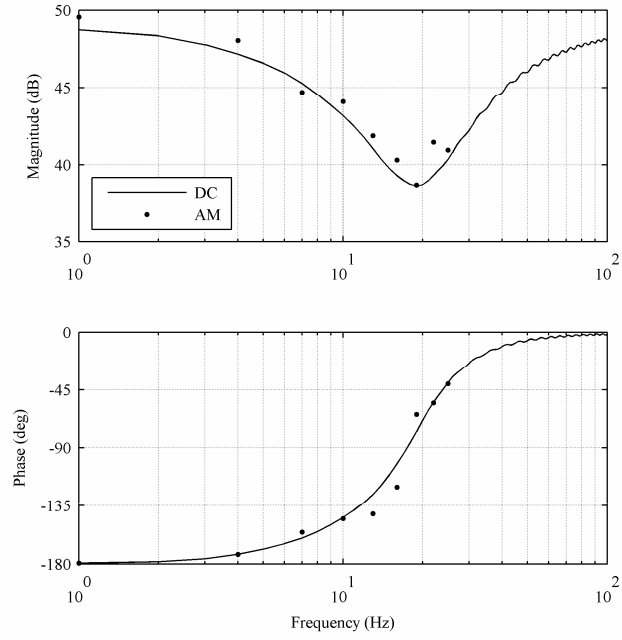


Figure 4.13. *Low frequency DC input impedance and amplitude modulation response.*

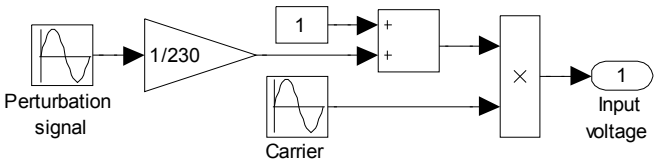


Figure 4.14. *Input voltage amplitude modulation.*

As may be obvious, the amplitude modulation (AM) response corresponds to DC-response. As was already mentioned in Section 2.3, the double averaged model gives the response to amplitude modulation, also referred as envelope impedance. Basically the averaging over the line cycle means the usage of input voltage RMS-value instead of the sinusoidal AC voltage. The higher frequencies are not simulated due to lack of any input filtering in the model. Thus the high frequency response would differ compared to measurements. A basic EMI filter with resonant frequency approximately a decade before the switching frequency would be easy to attach to the model but it really does not give more value to simulation results. The effect of LC-type input filter can be seen in the responses of measured loads. It is needed to suppress the high frequency noise to comply with radiated emission standards.

If the input impedance is simulated by its definition using various input voltage frequencies without amplitude modulation, the input impedance bode-plot would seem resistive where current loop is able to track its reference. If the PFC is assumed to be able to track the reference at low frequencies, the phase difference between input voltage and current is zero at those frequencies and impedance magnitude corresponds to input power. The low frequency magnitude with amplitude modulation corresponds to the input power at carrier frequency, i.e. if the DC power and power using carrier frequency input are the same, the magnitude plots should be exact. Information must be missing from the existing models because simulation with amplitude modulation shows the negative incremental resistance associated with instability but is not actually the input impedance. On the other hand, the input impedance can not be resistive at low frequencies even if the voltage and current were in phase because the current does not drop with the voltage by Ohms law.

5. FULL WAVE DIODE RECTIFIER

The diode rectifier is the cheapest and most simple rectifier. It consists only of passive components as shown in Figure 5.1. The diodes conduct and the capacitor is charged while the input voltage is higher than the rectified DC voltage (i.e. at the peaks of input sine wave). The output is a DC voltage slightly smaller than the peak value of input sine wave. Output ripple depends on the size of the output smoothing capacitor and output power. The problem with a diode rectifier is its highly nonlinear operation which leads to large harmonic currents, high THD and poor power factor.

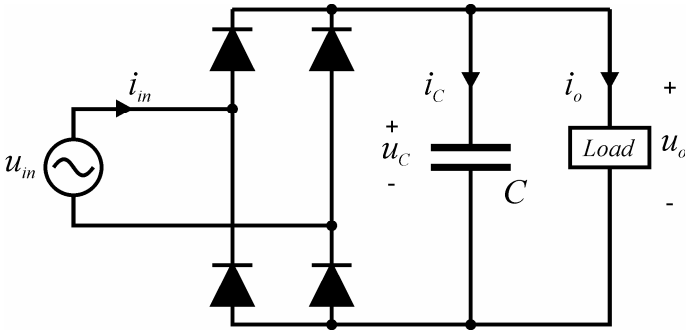


Figure 5.1. *Basic full wave diode rectifier circuit.*

Due to sinusoidal input voltage, the conventional small-signal linearization technique can not be used to derive analytical model for diode rectifiers. Not many reports have been published on the input impedance modeling of diode rectifiers. In [45], a model for input impedance was constructed applying the method of impedance mapping. In this thesis no analytical models are constructed but a simulation model for the circuit is build to study its behavior under various load conditions and capacitor sizes.

5.1. Simulink Model

Diode rectifier circuit is really simple and it could easily be built with various circuit simulation tools like PSPICE. A Matlab/Simulink model is built to benefit from other powerful tools available in Matlab. Compared to Figure 5.1, the supply network impedance (R_s and L_s) and parasitic resistances for diodes and capacitor are added. U_D is diode forward voltage drop. The elements of diode are multiplied by two since two diodes conduct at a time.

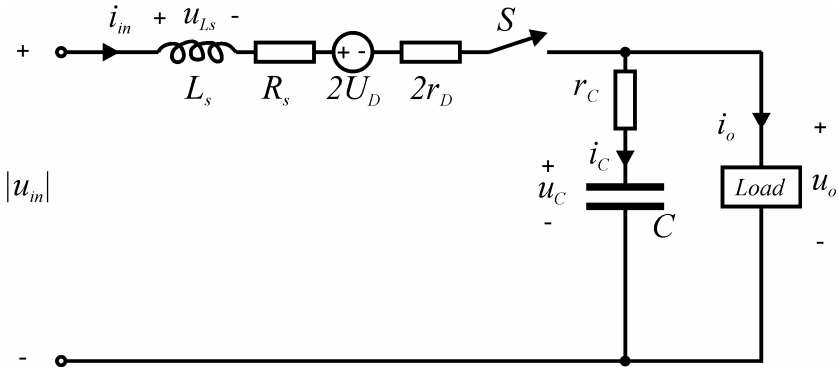


Figure 5.2. *Circuit used to build simulation model for diode rectifier.*

From Figure 5.2, on-time (5.1) and off-time (5.2) equations can be extracted. The switch is on when the voltage on the anode is higher than the voltage on the cathode of diode.

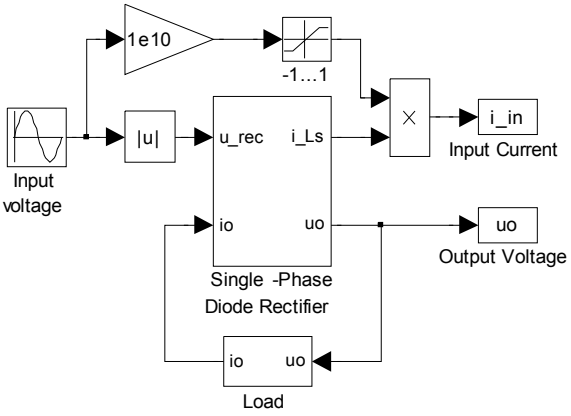
$$\begin{aligned} u_{L_s} &= u_s - (R_s + 2r_D)i_{L_s} - u_o - 2U_D \\ i_C &= i_{L_s} - i_o \\ u_o &= u_C + r_C i_C \\ i_{in} &= i_{L_s} \end{aligned} \tag{5.1}$$

$$\begin{aligned} u_{L_s} &= 0 \\ i_C &= -i_o \\ u_o &= u_C + r_C i_C \\ i_{in} &= 0 \end{aligned} \tag{5.2}$$

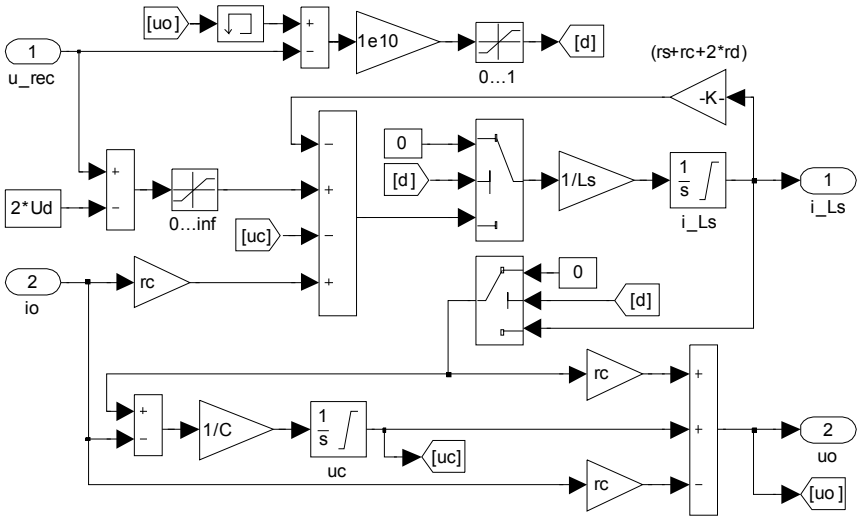
Equations (5.1) and (5.2) can be presented in state-space form as shown in (5.3) and (5.4), respectively. The Simulink model in Figure 5.3 is built based on these equations.

$$\begin{aligned} \frac{di_{L_s}}{dt} &= -\frac{(R_s + 2r_D + r_C)}{L_s} i_{L_s} - \frac{u_C}{L_s} - \frac{2U_D}{L_s} + \frac{u_s}{L_s} + \frac{r_C}{L_s} i_o \\ \frac{du_c}{dt} &= \frac{i_{L_s}}{C} - \frac{i_o}{C} \\ u_o &= r_C i_{L_s} + u_C - r_C i_o \\ i_{in} &= i_{L_s} \end{aligned} \tag{5.3}$$

$$\begin{aligned} \frac{di_{L_s}}{dt} &= 0 \\ \frac{du_C}{dt} &= -\frac{i_o}{C} \\ u_o &= u_C - r_C i_o \\ i_{in} &= 0 \end{aligned} \tag{5.4}$$



a) The overall model.



b) Single-phase diode rectifier.

Figure 5.3. *The simulation setup for diode rectifier.*

The absolute value of the input sine wave is transported to the diode rectifier block (as in Figure 5.2) in Simulink model shown in Figure 5.3. Input current can be calculated by multiplying the inductor current with sign of the input voltage. Output current can be calculated from the output voltage for desired load conditions. The model was verified with PSPICE. The simulation results from PSPICE were extracted to Matlab and are shown in Figure 5.4 with the simulation results from the Simulink model. The supply network impedance is approximately the same as in the standard network used in the harmonic measurements defined in standard EN 61000-3-3. The simulation parameters are defined in Table 5.1.

Table 5.1. *Parameters used in verifying the Simulink model.*

u_{in}	R_s	L_s	U_D	r_D	r_C	C	R_{Load}
230V	400mΩ	80μH	0.7V	50mΩ	200mΩ	100μF	2000Ω

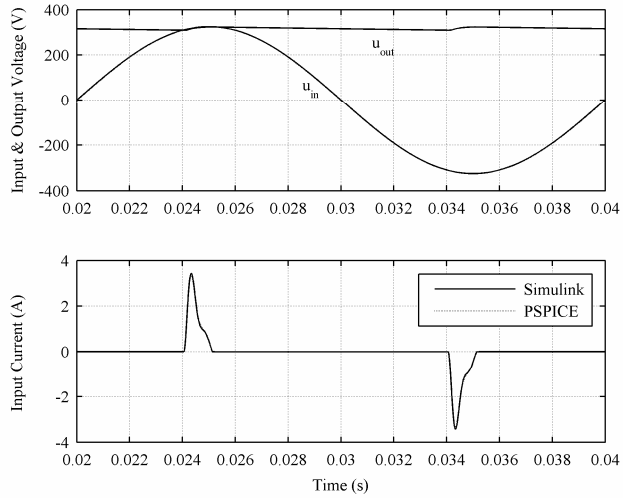


Figure 5.4. *Time domain simulation results for diode rectifier.*

The simulations are identical and therefore the model can be considered accurate. As can be seen, the input current is discontinuous and highly nonlinear, which makes analyzing the diode rectifier in frequency domain a difficult task.

5.2. Simulation Results

The shape of the input current depends on the capacitor, input voltage and load. The displacement factor is slightly capacitive and the inductor size effect to it can be seen from Figure 5.6. Large capacitors cause higher peak currents but the displacement factor is better. The phenomenon is easily explained with more energy loaded in the capacitor. The energy stored in the larger capacitor maintains the DC voltage longer and the conduction time starts nearer the input voltage peak. Also the voltage derivative is higher when the diode starts to conduct at the peak. Now the current shapes may be obvious when considering capacitor current equation ($i_C = C \cdot du_C / dt$). The simulated output voltages in Figure 5.7 are also clarifying.

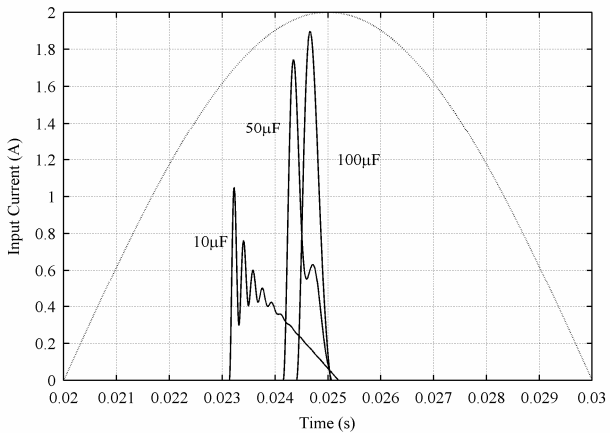


Figure 5.6. *The effect of capacitor size to input current with 230V input and 20W load.*

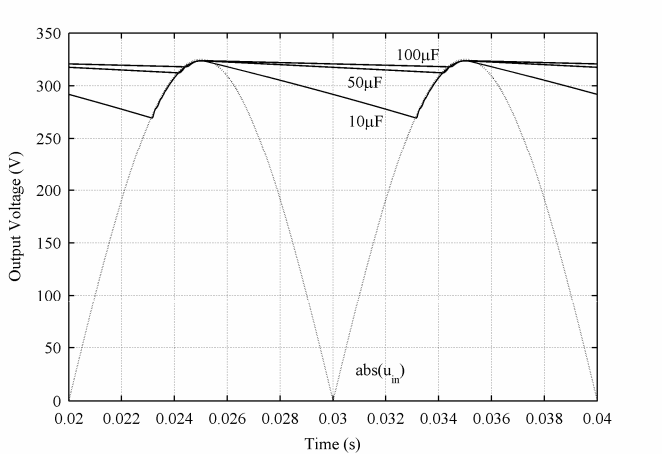


Figure 5.7. *The effect of capacitor size to output voltage with 230V input and 20W load.*

In Figure 5.8, the input voltage is increased from 115V to 230V during one millisecond. The dotted line represents the shape of the input voltage. Output power was 20W. It can be concluded that the overvoltage transients are more harmful with large capacitors but the displacement factor is better. The surge currents might cause damage to equipment or tripping of safety devices if not limited properly.

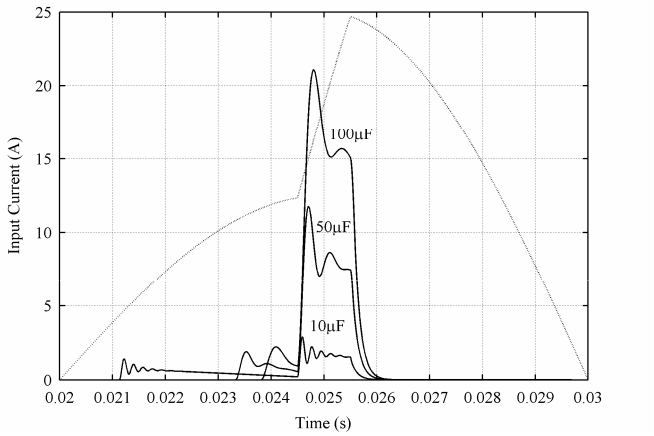


Figure 5.8. *Voltage-rise transients at peak of the input voltage.*

Figure 5.9 shows the simulated results during the voltage sags. At *t=0.04s* the voltage is dropped from 230V to 115V. The energy stored in the capacitor maintains the output voltage higher than the input voltage and the diodes do not conduct until the capacitor voltage reaches the input voltage level. The input current is clearly increased when the input voltage is lowered. Output power was 75W. Again the dotted line represents the shape of the input voltage.

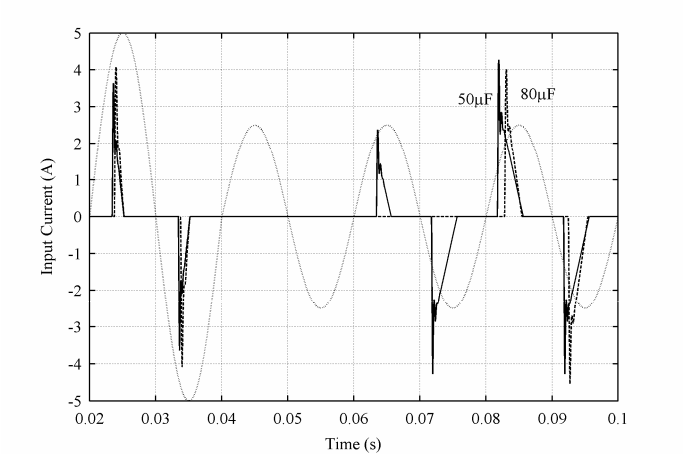


Figure 5.9. *A voltage drop simulation.*

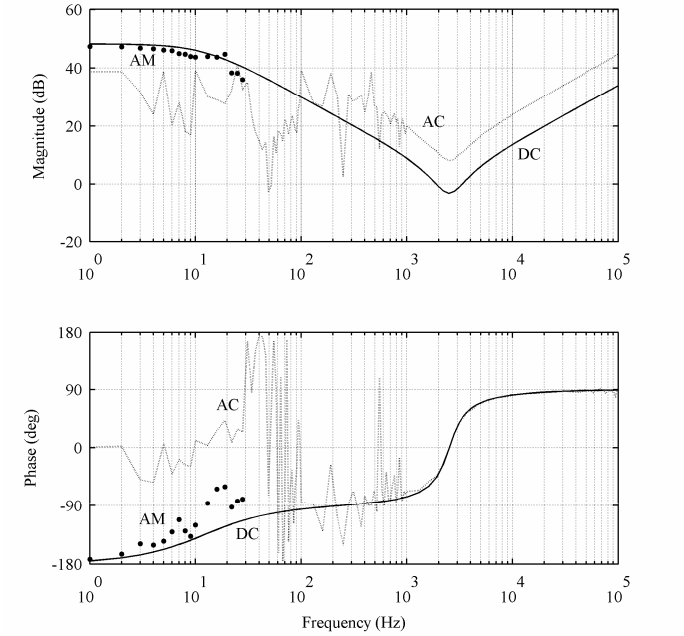


Figure 5.10. *Frequency responses with 50µF capacitor, 230V input voltage and 200W load.*

In Figure 5.10, the frequency responses from the input voltage to the input current based on simulations are presented. The solid line represents the input impedance simulated with DC input voltage and the dotted line is simulated with AC voltage. The dots represent response to the input voltage amplitude modulation. Again the amplitude modulation seems to correspond to DC impedance. Because the input power at AC and DC is the same and active power is delivered only by the fundamental components, it could be assumed that the DC response corresponds to the fundamental amplitude response. With AC input voltage the plot is readable at higher frequencies, where the line frequency harmonics are small enough to not interfere with the computations.

The resonant frequency 2.3 kHz of the simulated responses matches the inductance and capacitance values of 80µH and 100µF used in the simulations. It may be obvious that a voltage noise at the resonant frequency would cause excess current to flow. Such a noise voltage could be a consequence of PLC or other electronic loads connected in the point of common coupling.

6. PRACTICAL LOADS AND MEASUREMENTS

Energy saving lamps, laptop computer power supply and cell phone charger are subjected to practical measurements: the devices are measured at various input voltages in order to demonstrate their dynamic input characteristics. Time-domain voltage and current waveforms are recorded including the extraction of their Fourier components. The appearance of neutral currents in three-phase system is demonstrated connecting equal number of energy saving lamps in the phases. The input impedances are measured in frequency domain powering the devices with equivalent DC and AC input voltages. The DC characteristics are interesting also due to plans of using DC voltage in the commercial facilities [46]. The existence of the negative incremental resistance behavior is demonstrated by time-domain behavior also.

The power supply used in measurements was Elgar SW 5250A. Electrical characteristics were measured with Yokogawa WT1030 digital power meter, the oscilloscope was LeCroy Waverunner LT584M and Venable Model 3120 frequency response analyzer was used in frequency domain measurements.

6.1. Lighting Equipment

The most common lamp types are the traditional incandescent light bulbs and fluorescent lamps normally used in the offices and industrial lighting applications. The incandescent lamps are to be replaced by the energy saving lamps, which are also known as compact fluorescent lamps (CFL). In practice, the main difference is the power rating. The line voltage is rectified and the lamp circuit is fed from the DC source by high frequency resonant inverter [3] known as an electronic ballast (Figure 6.1).

The standard EN 61000-3-2 class C defines the harmonic limits for lighting equipment. The restrictions apply to all lamps with input power of over 25W. In practice, this means that an active PFC front end rectifier must be used if the input power exceeds 25W. Lower power limits can be attained with passive front end.

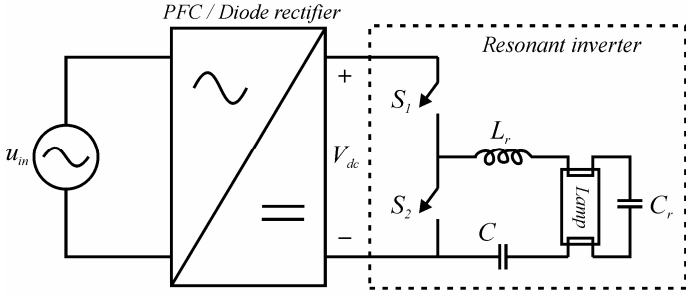


Figure 6.1. *Electronic ballast for fluorescent lamps.*

If the front end is implemented by using real PFC front, its low-frequency input impedance typically behaves as a negative incremental resistor due to the output voltage feedback. The resonant inverter works in constant-current mode which means that its input impedance should have capacitive nature. The fluorescent lamp behaves, however, as a negative incremental resistor and therefore, the input impedances could have the same feature.

6.1.1. Energy Saving Lamps

Energy saving lamps from five different manufacturers were used in measurements. The lamps are 11W rated, which should correspond to 60W incandescent lamps. Lamps were burned approximately 100 hours (3 hours on and 15 minutes off) before measurements in order to stabilize their behavior. There were three lamps from each manufacturer which were tested to have similar electrical characteristics. The test results are shown from one lamp and all the lamps were used in three phase system measurement. Negative displacement factor means that the reactive power is capacitive. The measurement results are listed in Table 6.1.

Table 6.1. *Measurements for 11W rated energy saving lamps.*

Manufacturer	U_{in}	I_{in}	*Fundamental*	*Displacement Factor*	*THD*	*Input Power*	*PF*
Airam	230V	79.9mA	56.2mA	-0.897	100%	11.6W	0.63
	200V	80.1mA	58.4mA	-0.878	93%	10.3W	0.64
	170V	83.7mA	64.0mA	-0.847	84%	9.2W	0.65
Biltema	230V	76.4mA	46.7mA	-0.899	129%	9.7W	0.55
	200V	73.9mA	46.8mA	-0.892	122%	8.4W	0.57
	170V	71.4mA	47.0mA	-0.883	114%	7.1W	0.58
Megaman	230V	75.6mA	52.3mA	-0.876	102%	10.6W	0.61
	200V	78.5mA	57.6mA	-0.851	92%	9.8W	0.63
	170V	72.7mA	54.6mA	-0.838	87%	7.8W	0.63
Osram	230V	78.7mA	52.0mA	-0.872	112%	10.5W	0.58
	200V	76.4mA	52.2mA	-0.862	106%	9.0W	0.59
	170V	75.1mA	53.6mA	-0.847	97%	7.7W	0.60
Philips	230V	79.0mA	52.7mA	-0.893	110%	10.8W	0.60
	200V	75.9mA	52.4mA	-0.882	104%	9.3W	0.61
	170V	73.6mA	52.9mA	-0.866	96%	7.8W	0.62

In the measurements, it took quite a long time for the input current to settle after voltage drop. The values were recorded when the current value did not change in one minute. This took approximately from 5 to 15 minutes. The explanation is the different amount of power dissipated to heat with different voltages and currents, which contributes to the

lamp temperature and its electrical properties. It can be seen from Table 6.1 that the input power drops with the voltage which was also noticed as a dimming of light output. The lamps manufactured by Megaman turned off approximately at 140V and on at 170V. The others turned off at 60-80V and on at 100-120V when voltage was slowly changed up and down. It was observed that the lamp was taking current even if it was turned off. The current and voltage waveforms for measured ESL's are shown in Figure 6.2. The harmonic content of the lamps is similar, therefore, only one is presented as an example in Figure 6.2.

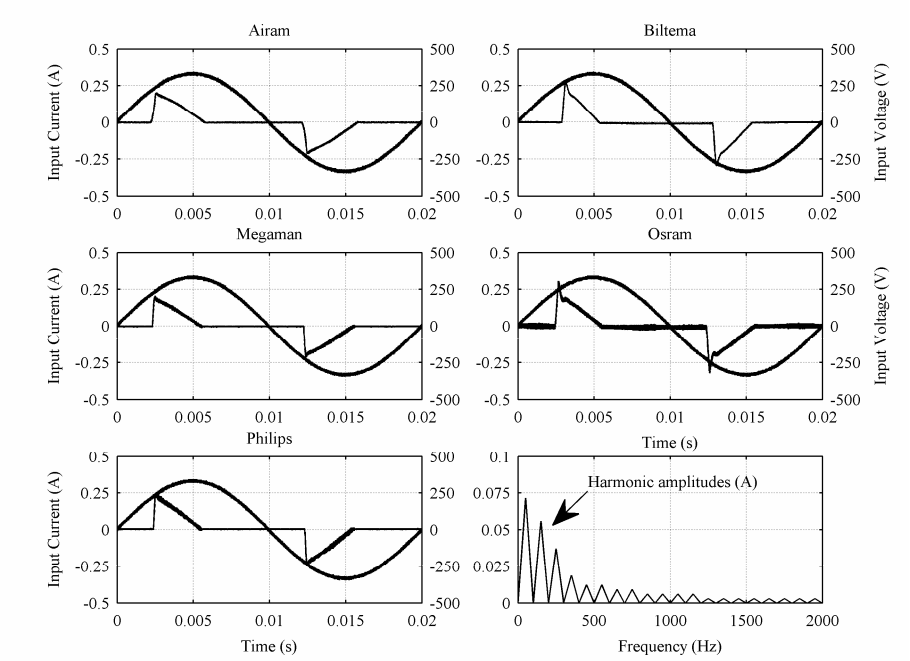


Figure 6.2. *Waveforms of energy saving lamps and harmonic content of the ESL manufactured by Philips.*

In three phase system the triplen harmonics of the line currents does not cancel each other as explained in Section 2.1. Figure 6.3 presents the line and neutral currents in three phase system with 5 lamps in each phase, one from each manufacturer. The harmonic content is presented for the phase 1 and the neutral conductor. The numerical values of the measurements are given in Table 6.2.

Table 6.2. *Three phase system measurements.*

	Phase 1	Phase 2	Phase 3	Neutral
I_{RMS}	0.373A	0.378A	0.370A	0.642A
THD	103%	104%	97%	22.3%
PF	0.63	0.62	0.64	-
Fundamental	0.255A	0.260A	0.264A	0.623A
Power	53.7W	53.9W	54.1W	-

The RMS current in the neutral conductor is approximately 1.73 times the line current and has the fundamental component of 150Hz as discussed earlier. The overheating of neutral conductor could have serious consequences if not sized properly.

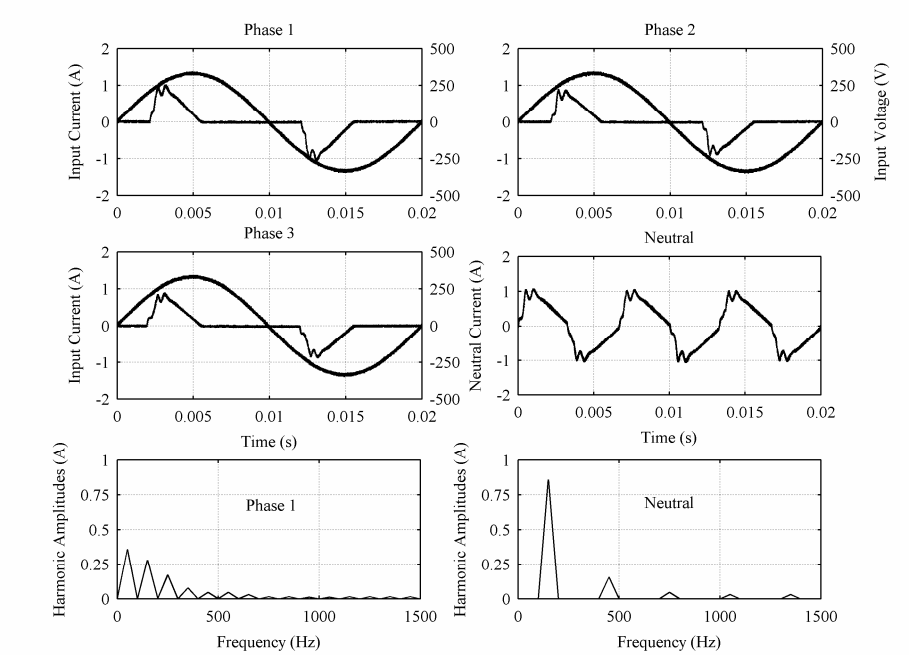


Figure 6.3. *Waveforms in three phase system with 15 energy saving lamps.*

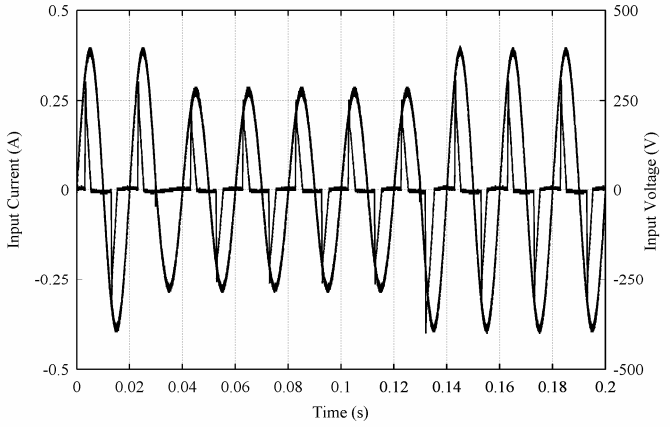


Figure 6.4. *Transient response of the ESL manufactured by Biltema.*

Figure 6.4 shows the transient response of the input current of the ESL without active PFC when the input voltage is changed from 260V to 200V and back. The diode bridge of the converter does not conduct during the first half cycle after the drop in the input voltage and consequently, the input current is zero but recovers during the next half cycle. When the voltage is increased back, the inrush current would take place. The voltage has changed at the zero crossing in Figure 6.4 and therefore the inrush current is quite small.

It is difficult to conclude based on the input current whether ESL exhibits negative-incremental-resistance like behavior or not due to the shape of the current. The frequency responses shown in Figure 6.5, when supplying the ESLs with DC voltage, show, however, that the negative-incremental-resistance like behavior would take place.

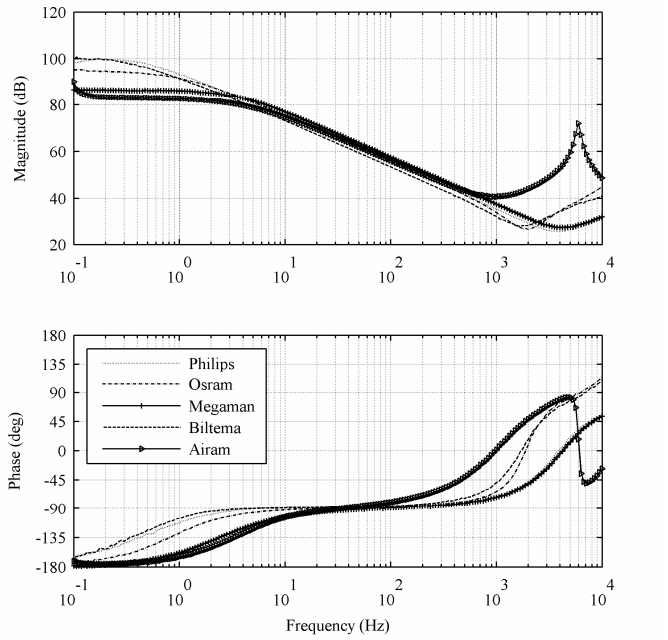


Figure 6.5. *Input impedances of ESL's with 230V_{DC} input.*

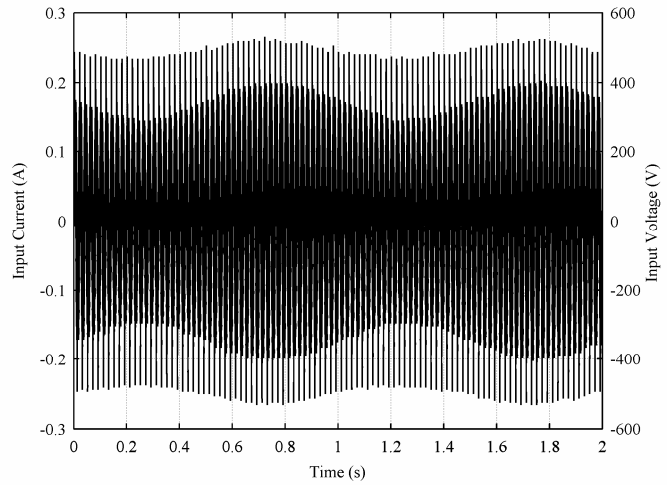


Figure 6.6. *1Hz amplitude modulation with an Airam ESL.*

Figure 6.6 shows the amplitude-modulated responses of the input current and voltage in time domain at 1Hz frequency. The time domain envelope responses indicate that the current and voltage are in phase but the information is misleading because the envelopes do not contain such information when the current is highly distorted. The frequency-domain measurement indicates that the low-frequency instability is possible if a proper LC-resonance takes place in the feeder system.

6.1.2. Electronic Ballast with PFC

ESL with PFC electronic ballast in the measurements was manufactured by Philips and it was driving two 95W T5 fluorescent lamps. The measured real power is surprisingly 10W lower or more than the rated power. The input current waveform is sinusoidal with superimposed switching-frequency ripple and power factor close to unity. The numerical measurements are shown in Table 6.3. The input voltage and current waveforms are shown in Figure 6.7.

Table 6.3. *The PFC electronic ballast measurements.*

U_{in}	I_{in}	*Fundamental*	*Displacement factor*	*THD*	*Input power*	*PF*
240	0.750A	0.738A	-0.990	6.5%	175.4W	0.974
200	0.896A	0.889A	-0.994	5.5%	176.9W	0.984
160	1.133A	1.190A	-0.997	10.9%	178.8W	0.986
150	1.153A	1.146A	-0.997	5.9%	171.5W	0.991
130	1.043A	1.033A	-0.997	7.9%	134.0W	0.988

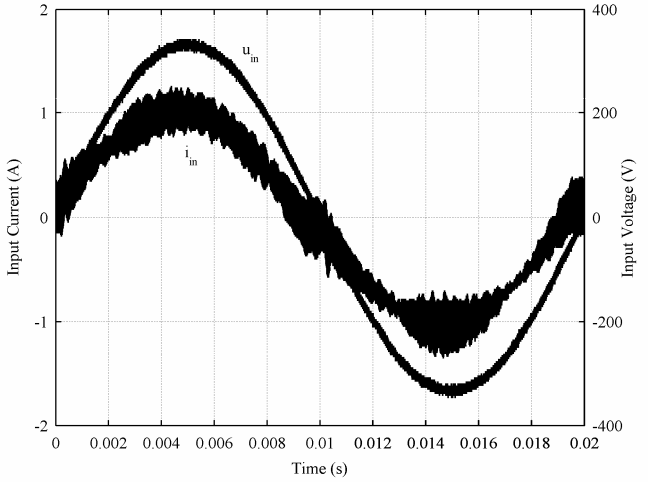


Figure 6.7. *Waveforms of the PFC electronic ballast.*

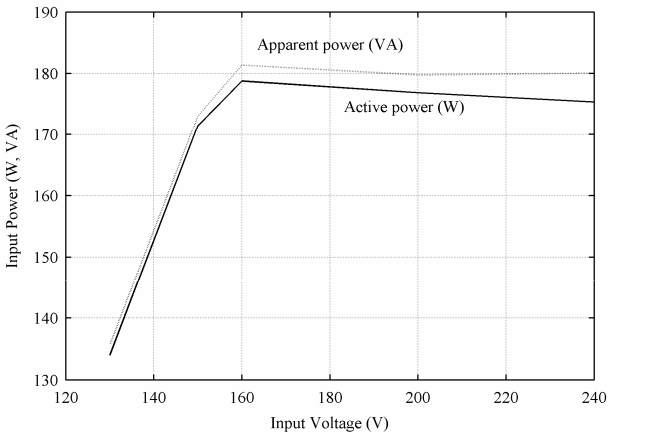


Figure 6.8. *Input voltage versus input power of the PFC electronic ballast.*

Figure 6.8 shows the measured input power in respect to the input voltage. According to it, the input power stays constant down to the input voltage of 160V after which the input power reduces and the lamp's light output also reduces. Figure 6.9 shows the time-domain response of the input current when the input voltage is dropped from 260V to 200V. It can be observed that the input current clearly increases when the input voltage decreases in order to maintain the constant input power, which is a clear indicator of the negative-incremental-resistance behavior in the input impedance. The impedance measurement at DC input voltage (solid line) and the amplitude-modulated AC input voltage (dots) supports clearly the same. The time-domain envelope responses of the input voltage and current shown in Figure 6.11 at 1Hz show also clearly that the voltage and current have a phase difference of 180˚.

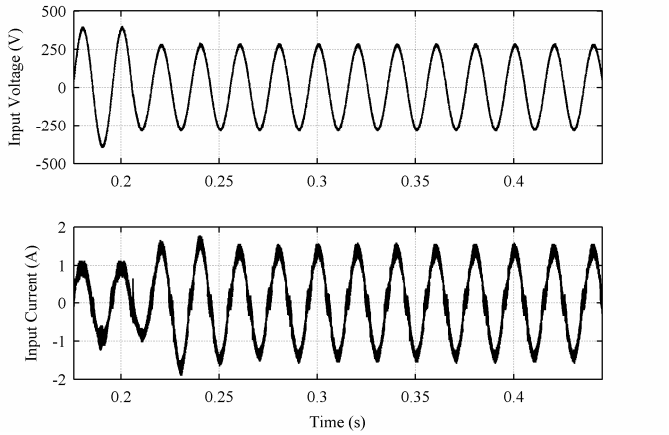


Figure 6.9. *Voltage drop with PFC electronic ballast.*

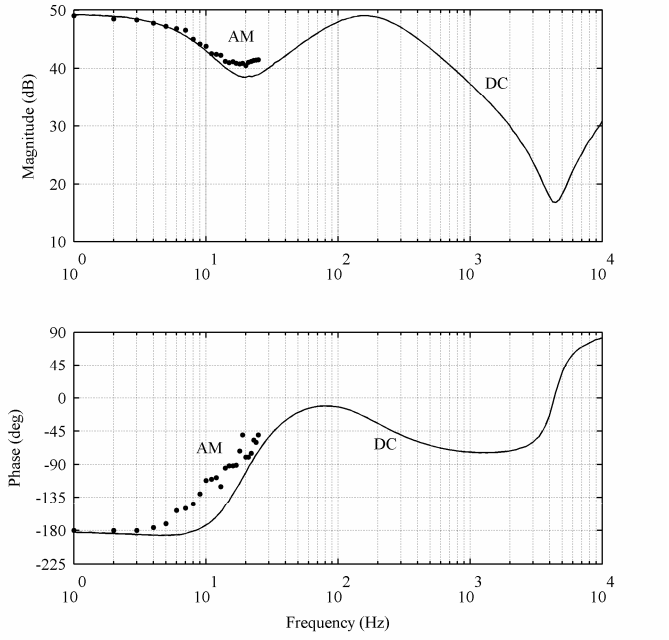


Figure 6.10. *Frequency response of PFC electronic ballast.*

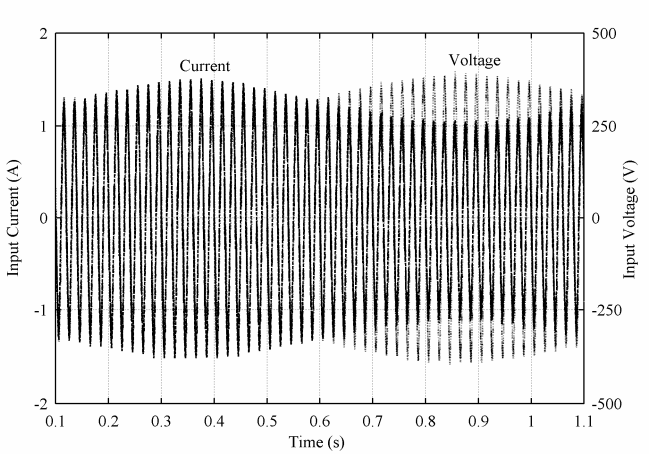


Figure 6.11. *Amplitude modulation at 1Hz with PFC electronic ballast.*

The PFC electronic ballast operates similarly to the simulations presented earlier in Chapter 4. The input current waveform is close to sinusform and the power factor close to unity. The harmonic content of the input current of similar electronic ballast is reported in [47]. It may be obvious that during the voltage dips the currents increases which may cause capacity problems in network if not considered properly when sizing the conductors. The small voltage transients do not easily cause flickering as is the case with incandescent lights. The PFC converter is clearly susceptible to low-frequency instability problems as reported to take place in [26, 29, 30].

6.2. Other Electronic Loads

The input voltage range of the electronic loads may be even from 80V to 270V which is known as universal input voltage range. Usually such electronic devices are the chargers of laptop computers and mobile phones as well as the power supplies of TV sets, etc. The use of the universal input voltage range is usually implemented for logistic reasons.

6.2.1. Laptop Computer Power Supply

The rated power of the power supply of a laptop computer is 65W and therefore the power factor correction is not mandatory (EN 61000-3-2 class A; ≥75W). The diode-rectifier with a smoothing capacitor supplies a DC-DC converter with tight output voltage/current regulation. Therefore the low-frequency input impedance would exhibit negative incremental resistor behavior. The input voltage range of the power supply is 100-240V. The measurements are done when the internal battery of the laptop is charging. The numerical results are given in Table 6.4.

Table 6.4. *Laptop computer power supply measurements.*

U_{in}	I_{in}	*Fundamental*	*Displacement factor*	*THD*	*Input power*	*PF*
230V	0.613A	0.155A	-0.975	108%	59.3W	0.42
110V	1.056A	0.541A	-0.957	149%	58.7W	0.47

Figure 6.12 shows the measured input voltage and current at the input voltage of 230V. The shape of the input current indicates that the smoothing capacitor is rather large yielding low reactive power but still high distortion power. The figure shows also that the half-cycle currents are unbalanced and consequently, the power supply injects DC current into the AC supply. The unbalance reduces when the input voltage is lowered towards the minimum input voltage level.

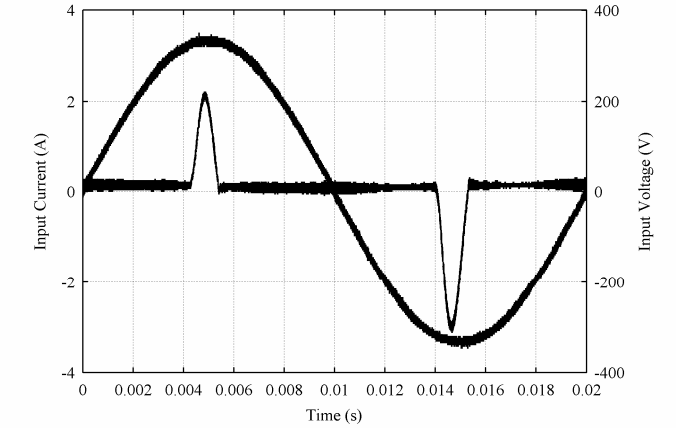


Figure 6.12. *The power supply waveforms.*

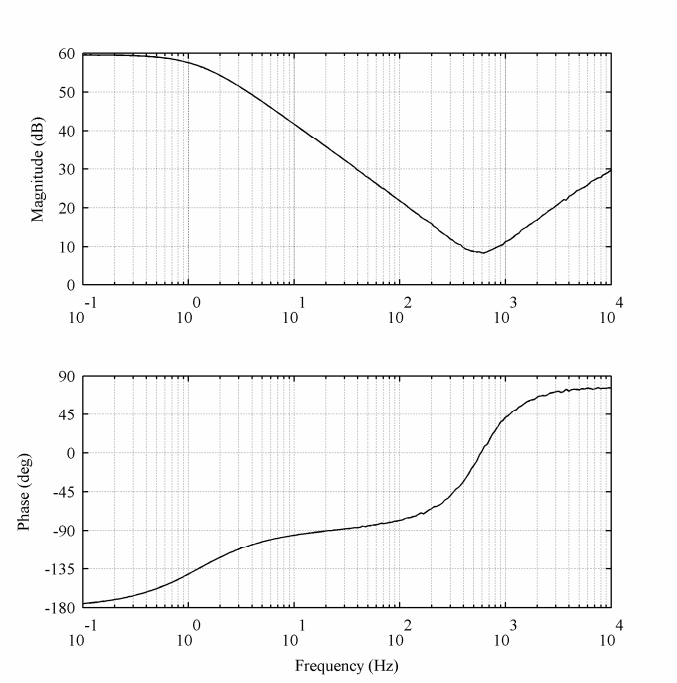


Figure 6.13. *Input impedance of the power supply with 230V_{dc} input.*

Figure 6.13 shows the measured frequency response of the input impedance when the input voltage is an equivalent DC voltage. The low-frequency behavior is as expected for the device due to the internal DC-DC converter.

6.2.2. Cell Phone Charger

An electronic cell phone charger with universal input voltage range was characterized. The front-end rectifier is similar as in all the low-power devices and the internal DC-DC converter is usually a flyback-type converter. The input voltage and current waveforms at high and low input-voltage conditions are shown in Figure 6.14. The shape of the input current reveals that the smoothing capacitor is rather small (see Figure 6.12 for comparison). The high-line input current indicates that the charger injects DC current into the input supply. The unbalance in the half-cycle currents is largely removed when the input voltage is lowered to the low line level. The numerical measurements are given in Table 6.5.

Table 6.5. *Cell phone charger measurements.*

U_{in}	I_{in}	*Fundamental*	*Displacement factor*	*THD*	*Input power*	*PF*
230V	0.059A	0.026A	-0.991	211%	5.6W	0.41
90V	0.109A	0.073A	-0.927	118%	5.7W	0.58

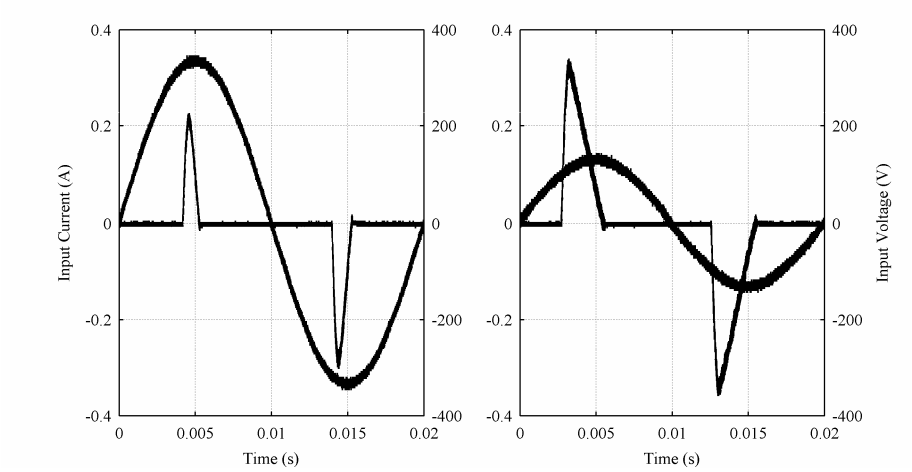


Figure 6.15. *Cell phone charger waveforms.*

The operation does not really differ from the laptop computer power supply measured in Subsection 6.2.1. Only the input power is smaller.

6.2.3. Diode Rectifier with Constant Power Load

A diode-rectifier-based front end was designed which operated at the AC input voltage of 50V and it was used to supply a switched-mode converter where the output voltage

was tightly regulated (i.e. a constant power load of 5W). The numerical measurements are provided in Table 6.6.

Table 6.6. *Diode rectifier measurements.*

U_{in}	I_{in}	*Fundamental*	*Displacement factor*	*THD*	*Input power*	*PF*
45V	0.379A	0.196A	0.953	165%	8.3W	0.49
35V	0.420A	0.246A	0.925	137%	8.0W	0.54

The measured input voltage and current waveforms are shown in Figure 6.15 at the input voltages of 45V and 35V with the corresponding input current harmonics. The input current at the input voltage of 45V shows unbalanced half-cycle currents and consequently, DC current is injected into the input supply. Figure 6.16 shows the measured frequency response of the input impedances at the input voltage of $40V_{DC}$ (solid line) and the phase of the input impedance at 0.5Hz and 1Hz measured by using amplitude modulation. The corresponding time-domain waveforms are shown in Figure 6.17. In this case, the envelope behavior matches the measured behavior under the DC input supply.

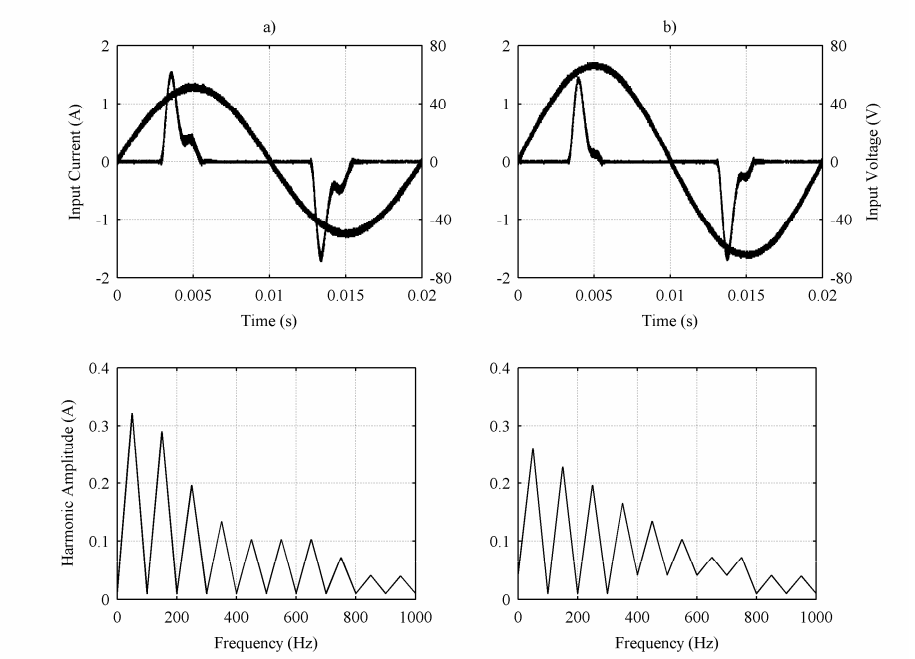


Figure 6.15. *Waveforms of diode rectifier with 100μF capacitor and 5W load (input voltage a) 35V and b) 45V).*

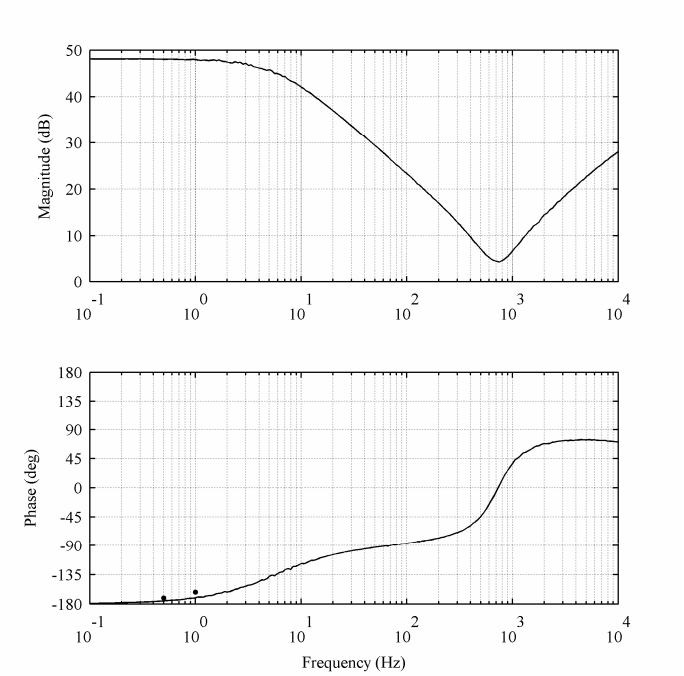


Figure 6.16. *Diode rectifier input impedance with $40V_{dc}$ input.*

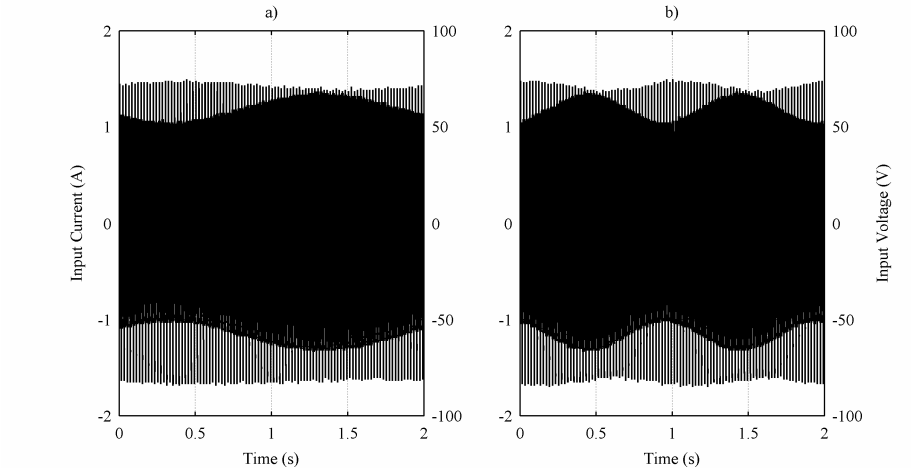


Figure 6.17. *Amplitude modulation at a) 0.5Hz and b) 1Hz.*

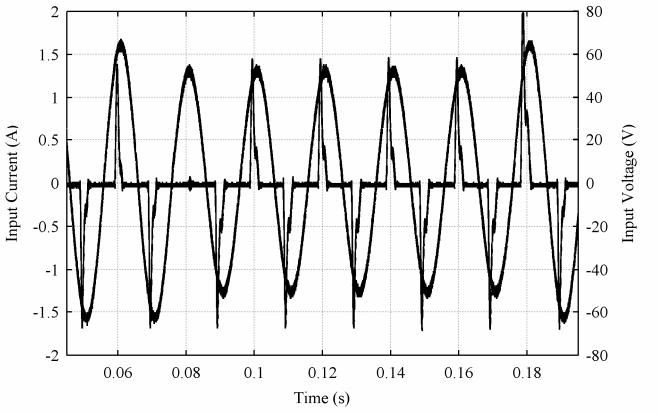


Figure 6.18. *Transient response for diode rectifier.*

Figure 6.18 shows the input current behavior when the input voltage is dropped from 45V to 35V and back. The dynamic behavior is similar to shown earlier in Section 6.1.1.

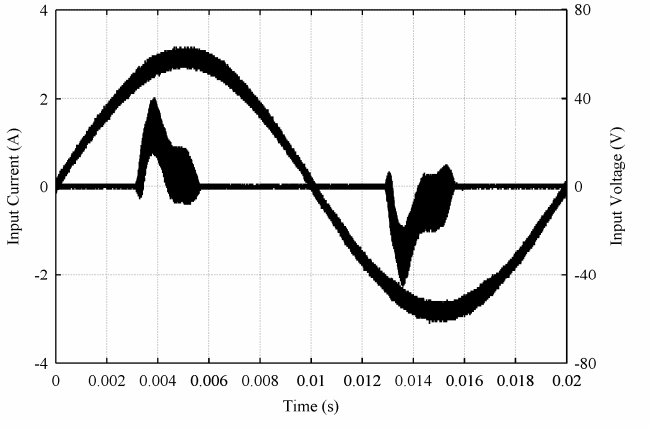


Figure 6.19. *Input current with input voltage containing a 75kHz component.*

Figure 6.19 shows the input current and voltage when a 75kHz voltage signal was superimposed on the supply voltage for demonstrating the possible effect of PLC applications.

7. CONCLUSION

The thesis investigated the interactions the electronic loads connected into the grid may cause. The main focus has been on the energy saving lamps, which are to replace the conventional incandescent lamps by 2013. In addition, a power supply of a laptop computer and a charger of a mobile phone were characterized.

Tight competition especially in the consumer business stipulates that all the products have to be designed in terms of lowest possible costs. This means that the compliance to the relevant standards is fulfilled with minimal margins and the lowest requirements level is absolutely adopted in use. This affects especially the injection of harmonic currents into the grid: The standard concerning the lighting equipment sets low limits, easily achieved with passive front end, for the equipment with rated power less than 25W. The most usual incandescent lamp to be replaced is 60W which can be replaced with an 11W energy saving lamp. The power limit for TV sets, laptop computers, mobile phone chargers, etc., under which no limitations are applied is 75W.

As a consequence of this, an excess amount of apparent power is taken from the grid adding voltage losses and causing excess heating of transformers, inductors and capacitors. In addition, the sum of phase currents in a three phase system does not anymore sum to zero but the neutral current increases and can reach the level of 1.7 times the phase current. This may be a severe problem when the neutral conductors are typically sized equal or less than the line conductors. It was also observed that there may exist half-cycle asymmetry in the input current of the electronic loads based on the simple diode rectification. The asymmetry means that DC current is injected into the grid which may saturate transformers and inductors when large amount of such devices is connected into the grid. The cause for the appearance of the asymmetry may be the unbalance in the diode losses. The asymmetry typically reduced when the input voltage was lowered to the minimum input voltage and was the worst at the high input voltage.

Logistically optimal design in terms of the input voltage may be such that the product can be used globally without any concern of the input voltage. Such an input voltage range is known as universal input ranging from 80-270V in a single-phase system. As a consequence, the electronic loads may be operative during the deep voltage sags with substantial increase in grid current which may cause problems where the grid supplying ability in terms of current is not anymore sufficient and stability problems may occur. Another source of stability problems in the electronic loads is their low-frequency input impedance which tends to behave as a negative resistance due to the tight regulation of their output parameters or the behavior of the compact fluorescent tubes. The stability problems may occur when a LC-resonance in the grid occurs at the

frequencies where the negative resistance feature dominates the input impedance of the electronic loads.

Automatic meter reading (AMR) of the consumer electricity consumption is becoming a part of everyday life. AMR is accomplished by using technique known as power line communications, where high-frequency carrier signals on the top of the voltage will be injected into the grid. Those high-frequency voltage signals may cause high-frequency currents to appear due to the capacitors inside the electronic loads. The same capacitors may also create high-frequency resonances in conjunction with the network inductances. If the network voltages contain frequency components at the resonant frequencies, high resonant current may appear. The existence of a large amount of different frequency components is probable because of the switching frequencies of the electronic loads. These high frequency signals and the resonances may also disturb the data transfer in the power line communication and cause severe problems for the implementation of AMR.

The replacement of the incandescent bulbs with the energy saving lamps may be well reasoned from the climatic perspective but the new problems appearing from the use of the energy saving lamps may actually exceed the benefits and make the justification questionable. The situation can be improved by tightening the regulations limiting the injection of harmonic currents into the grid but it would actually increase the probability of network wide instability to take place endangering the everyday life of electricity-dependent societies.

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